Design and Analysis of 4- Bit Binary Synchronous Counter by Leakage Reduction Techniques

Himal Pokhrel[#1], Deepak Kumar[*2], Anjali Sharma[#3]

[#1,*2] MSC (Physics) Student, Department of Applied Sciences, Shimla University, H.P., India
[#3] Assistant Professor, Department of ECE, Shimla University, H.P., India

Abstract: *Counter is one of the fundamental and essential components used in most of the digital devices. Design of power efficient counter design has become essential for the researchers. In leakage dominant technologies, leakage current increases for traditional CMOS structures due to the reduction in threshold voltage. The increase in leakage current due to voltage scaling causes increase in static power dissipation. Various techniques have been implemented by the researchers to design counters which would consume the lowest power possible. In this paper, we have presented a design of 4 - bit binary synchronous counter using three different techniques namely CMOS technique, Sleepy transistor technique (STT) and Forced stack technique (FST). The circuit designing and parametric analysis has been carried out using microwind 3.1 and DSCH 3.1 software on 65nm technology. The height, width, surface area and power consumption in the case of all the three techniques have been measured at three different supply voltages i.e. 0.5V, 0.7V and 0.9V respectively. It is found that, the power consumed by FST counter and SST counter is much less as compared to power consumed by CMOS counter. The average power reduction is 44.9% in the case of sleepy transistor technique and the average power reduction is 70.1% in the case of FST as compared to CMOS counter. Although these techniques are power efficient as compared to CMOS technique but this is on the expense of larger surface area. Counter designed by these techniques can be useful where low power requirement will be primary concern.*

Keywords — *CMOS, DSCH, FST, Leakage Power, Microwind, Synchronous Counter*

I. INTRODUCTION

A digital counter circuit consist of two or more flip flops with combinational elements. The flip flop change state in a prescribed sequence. It is used to counts the number of occurrence of an event or input signals. Counter has wide range of application in several circuits like signal generators, microcontroller, digital memories digital clock and timing circuit [1]. High performance computers with low power consumption are in need for all designers. In CMOS technology high density and high performance can be achieved by scaling down features size and threshold voltage. Due to decrease in features size, channel length becomes shorter and this causes increase in sub threshold leakage current through a transistor during its off mode. So, the static power consumption increases. This is also called leakage power dissipation which has been increasing significantly compared to the total power consumption [2].

For CMOS circuit the total power dissipation includes dynamic and static components during the active mode of operation. The dynamic (switch) power and leakage power are given as:

$$P_D = \alpha f_c V_{DD}^2 \quad (1)$$

Where α = Switching activity, f = Operation frequency, C = Load capacitance, V_{DD} = Supply voltage

Leakage power is given by

$$P_{Leakage} = I_{Leakage}.V_{DD} \quad (2)$$

In CMOS inverter, current flows from source to drain when $V_{GS} > V_T$. In real transistors current does not abruptly cut off - below threshold, but drops off exponentially. This condition is known as leakage conduction and result in undesired condition when transistors are normally off. The leakage current is the sub threshold or weak inversion current that flows from drain to source of transistor when it is off (i.e. $V_G < V_{tb}$). Leakage current drawn from the circuit when threshold voltage becomes greater than the gate to source voltage, is given by equation (3). So current can be decreased by increasing the threshold voltage and substrate voltage, reducing the gate source voltage, drain source voltage and temperature.

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nv_T}} \left\{ 1 - e^{\frac{-V_{ds}}{v_T}} \right\} \quad (3)$$

Where I_{ds0} = Current at threshold, V_t =Zero bias threshold swing coefficient, n =Sub threshold swing coefficient, V_T = Thermal Voltage.

In this paper, we have implemented the most important techniques namely CMOS technique,

Sleepy technique and Forced Stack technique in order to design 4- bit Synchronous Counter and studied its power consumption for various supply voltage. The main purpose of doing this is to compare the power consumption in different techniques and analysis the cause why a particular technique consume less power. This will ultimately motivate the researcher to designs for new lesser power consuming circuit especially the circuit that reduces leakage power or the static power consumption [3-4].

II. Review of Previous Researches

This section briefly discusses the review of some previous counter circuits designed by different techniques on different technologies. Shilpa Shrigirieet. et. al. designed a 16- bit binary counter implemented with clock gating at 4- bit level . They compared power consumption between the counter implemented with clock gating and the one with normal implementation. It was found that there was a reduction of power by 61.12%. For a normal counter they connected four-four bit counter blocks are stitched together using the clock gating logic. The clock gating logic for the any stage fed through AND function signal from previous stage. The NXT-AND acts as enable signal for normal counter and same acts as gating signal for clock gating counter [5]. Praween Sinha et. al. designed a four bit binary counter using enhancement type MOSFET. They designed T-flip flop using an X-OR gate and D-flip flop were connected with the help of AND gate to make a 4-bit binary counter. This counter worked at voltage of 3V. It has maximum clock frequency of 476 MHz, maximum rise and fall time was 2.1ns and 2ns. It showed reduced power consumption and better output signal level [6].

Calvignac Yvan et. al. have designed and simulated a 4-stage binary counter by CMOS techniques on 65 nm technology using Microwind and DSCH 3.1 Software. They cascade four D register to make 4-stage counter. Each D register was formed by connecting two D flip flop and a NOT gate [7]. Sandeep Thakur et. al. designed and simulated 4-bit ring counter using 45 nm technology. They designed a master slave D flip flop using NAND gate and an inverter and four D flip flop were cascade to forming counter. Flip flop were provided with same clock pulse to because of synchronous nature of ring counter. The designed the counter using cadence EDA tool. They simulated the designed ring counter for 200ns and analysed using 45 nm technologies at 1 voltage rating in cadence tool. The delay & power dissipation of the proposed design was compared with that of conventional design. The transistor count, delay and power dissipation were found to be respectively 106, 120.125ns and 313.43pw for conventional ring counter and 58, 5.216ns and 219.85 pw for proposed ring counter [8].

III. The Proposed Counter

We have designed 4- bit synchronous counter by using three different techniques i.e. CMOS Techniques, Sleepy Transistor technique and Forced Stack technique. A 4-bit counter consists of four D-registers, connected in series along with four X-OR gates and three AND gates as shown in Fig. 1. The clock pulse is provided to each D-register simultaneously. Output of each AND gate act as an input to next cascade AND gate and output of XOR gate act as an input to D- register. Output of 4-bit counter has been displayed on hexadecimal display.

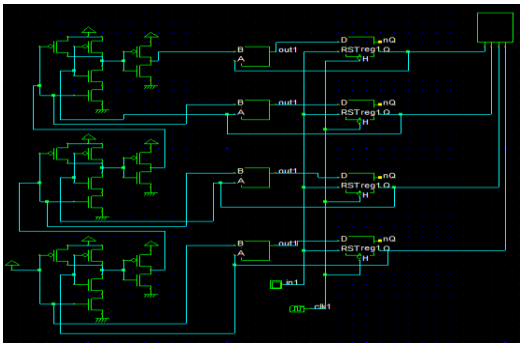

Fig 1: 4-bit counter Design

A. Layout Design of X-OR gate

We designed X-OR gate using CMOS .In all three methods the basic building blocks are NMOS and PMOS. The difference is in their arrangement and number. The circuit diagram and layout design of X-OR using CMOS technique is shown in Fig. 2 and 3 respectively.

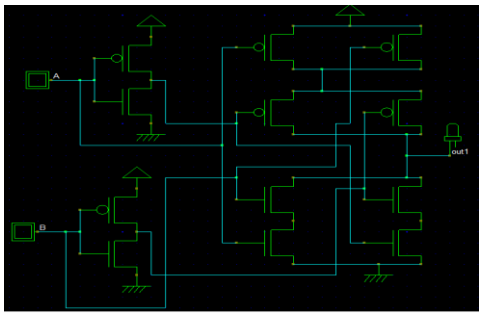

Fig 2: CMOS XOR Gate

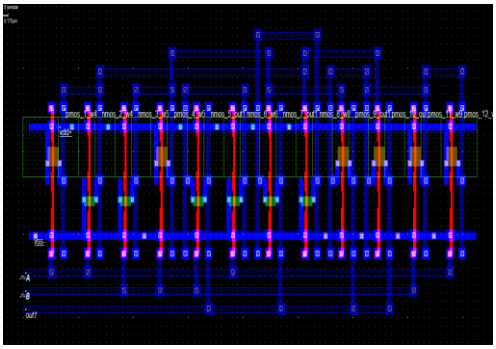

Fig 3: Layout of XOR Gate

B. Simulation for X-OR gate

We simulated XOR gate using Microwind 3.1 on 65nm technology. Foundry voltage at 65nm is 0.7V. XOR gate designed by CMOS shows full voltage swing at the output. Parametric analysis has been carried out at 5nm scale. Post layout simulations of XOR gate has been shown in Fig. 4.

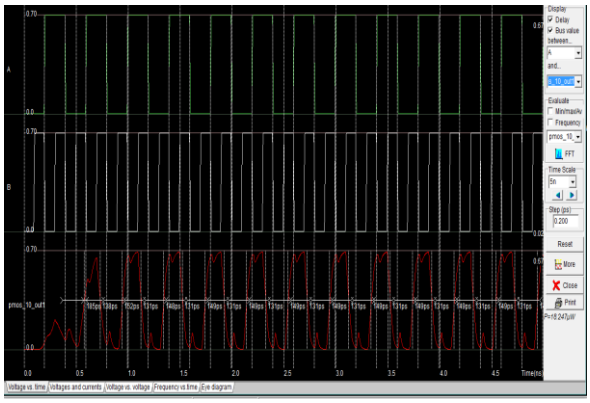

Fig 4: Post layout simulations of XOR gate

Circuit diagram and Layout of XOR gate using Sleep Transistor Technique (STT) is shown in Fig. 5 and 6 respectively. This circuit has been designed by using 8 PMOS and 8 NMOS transistors.

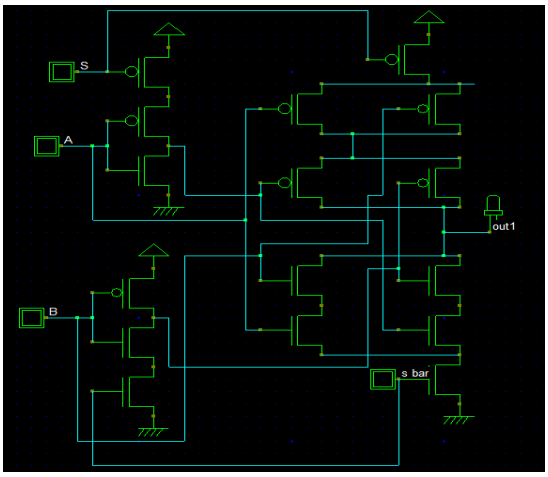

Fig 5: XOR gate using Sleep Transistor Technique

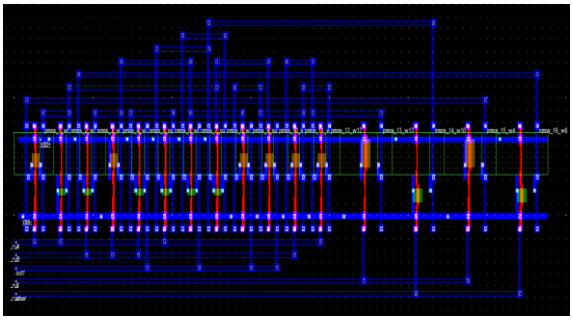

Fig 6: Layout of XOR gate by STT

Circuit structure of STT is shown in Fig.7 which consist CMOS implementation for actual logic implementation and two high threshold transistors as sleep transistors.

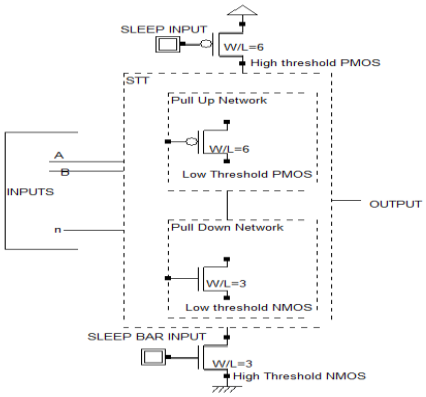

Fig 7: Circuit Structure of STT

C. D-flip flop

D flip flop, also called Data flip flop or Delay flip flop is constructed from a gated SR-flip flop with an inverter added between S & R inputs to allow for a single D (Data) input. This single data input is used to replace "SET" signal and the inverter is used to generate the complimentary "RESET" input there by making a level sensitive D type flip flop. The block diagram of D flip flop using NAND and NOR gate is shown in Fig. 8.

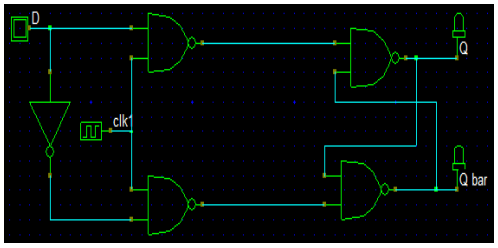

Fig 8: D- FF using NAND Gate

We designed D flip flop has been designed by using all three mentioned techniques. D flip flop's module was formed and simulated so that it can be used for designing counter circuit. The circuit design of CMOS D flip flop is shown in Fig. 9.

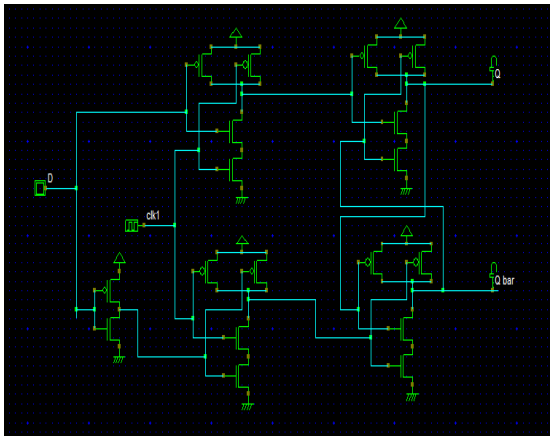

Fig 9: C*ircuit design of CMOS D flips flop*

After studying the design and implementation of D flip flop, we extracted similar module of D register from the symbol box in the Microwind3.1 and constructed a 4-bit synchronous counter.

IV. 4-BIT SYNCHRONOUS COUNTER: DESIGN AND WORKING

The basic block diagram of 4-bit synchronous counter is shown in Fig 10. The counter module consist of 4 XOR gates, 3 AND gates and 4 D FFs. Output of each XOR gate act as an input to the cascaded D FF. Output of the module cam be observed by hexadecimal display.

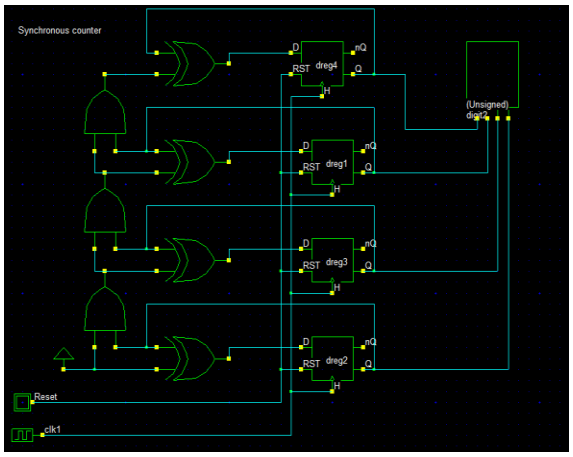

Fig 10: *B*asic block diagram of 4-bit synchronous counter

The circuit diagram of 4-bit synchronous counter by CMOS technique is shown in Fig. 11 and corresponding layout is shown in Fig. 12. All modules are connected in the same way as shown in Fig. 10. To reduce the circuit complexity XOR gate and D FF module has been used which is designed by the CMOS technique only.

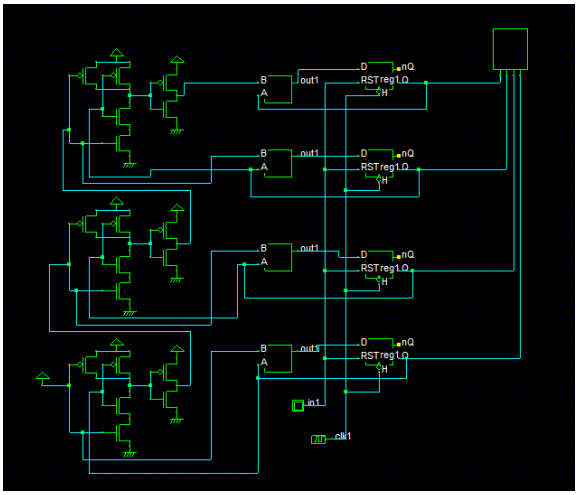

Fig 11: 4-bit synchronous counter by CMOS

The layout design and post layout simulations for CMOS counter are shown in Fig. 12 and Fig. 13.

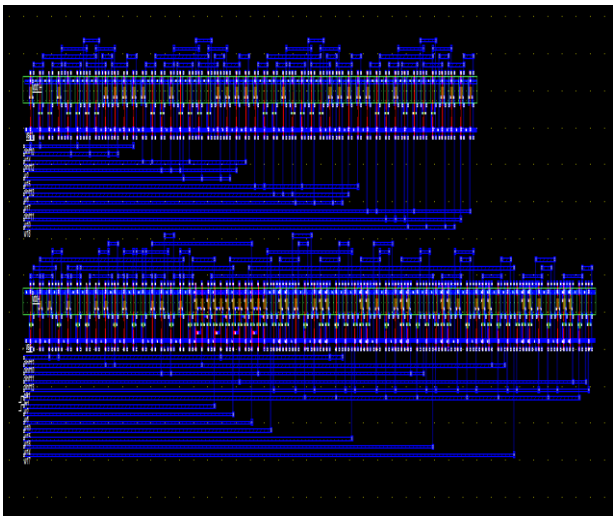

Fig 12: Layout of 4-bit synchronous counter by CMOS

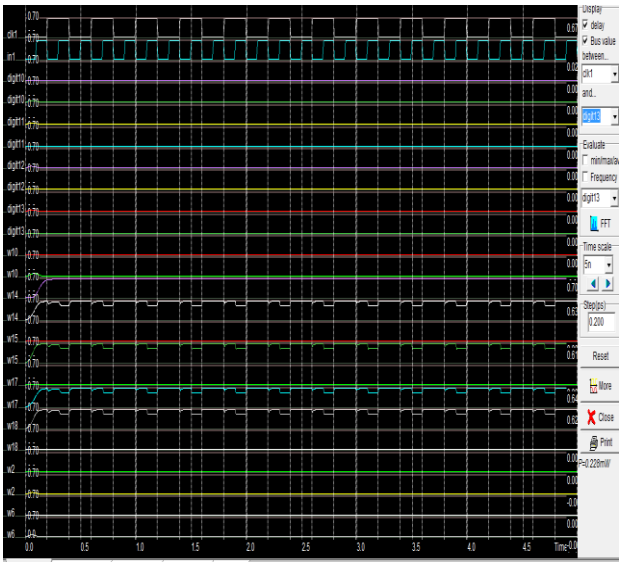

Fig 13: Post Layout simulations of 4-bit synchronous counter by CMOS

Similarly the circuit diagram of 4-bit synchronous counter by STT and FST are shown in Fig. 14 and 15 respectively.

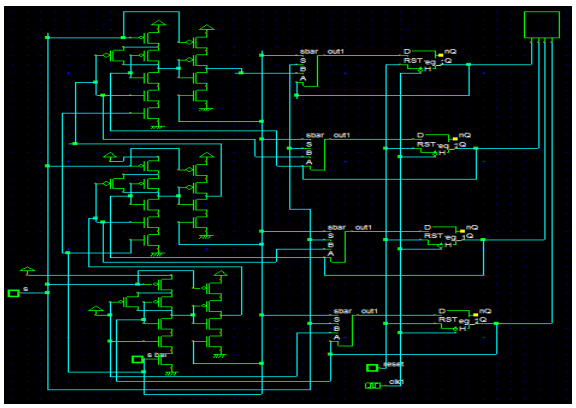

Fig 14: C by STT

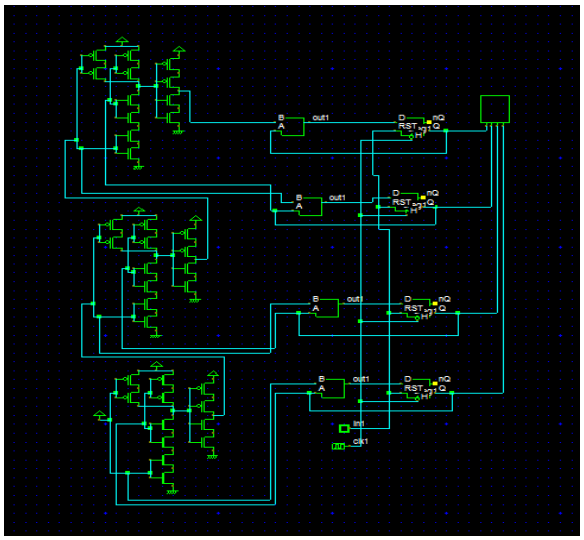

Fig 15: 4-bit synchronous counter by FST

V. Result and Discussion

We designed 4-bit synchronous counter using CMOS technique, Sleepy Transistor Technique and Forced Stack Technique. The layout design and simulation result of all three counters were obtained. We measured number of PMOS, number of NMOS, Height, Width and Surface Area of XOR gate and synchronous counter in all three cases.

TABLE I: Layout result of X-OR Gate

Technique	PMOS	NMOS	Height (µm)	Width (µm)	Area $(\mu m)^2$
CMOS	6	6	6.0	14.5	87.2
STT	8	8	8.3	23.7	197.7
FST	12	12	7.2	28.3	203.4

TABLE III: Layout result of 4-bit Synchronous counter

Technique	PMOS	NMOS	Height (µm)	Width (µm)	Area $(\mu m)^2$
CMOS	69	77	19.9	70.7	1405
STT	107	115	39.9	71.1	2836.3
FST	102	110	314	74.5	2304

The Table-I gives height, width and surface area along with number of PMOS and NMOS for X-OR gate designed by three different techniques and the second Table-II shows the relative number of PMOS and NMOS, Height, Width and Surface area of the designed counter for different techniques.

The ratio of width and length for PMOS and NMOS are taken 6 for PMOS and 3 for NMOS in case of CMOS technique and STT, whereas for circuit design by FST the ratios are 3 and 1.5 for PMOS and NMOS respectively. We keep length constant i.e. equal to 0.07µm and choose the appropriate value of width for different techniques. The value of width is 0.42µm and 0.21µm for PMOS and NMOS in CMOS technique, 0.21µm and 0.105µm in FST respectively. The added Sleep and Sleep bar NMOS and PMOS in STT have width and length just double of that in normal CMOS.

From the comparison tables it can be observed that the number of transistors as well as surface area increase as we go from CMOS technique to FST. Hence FST requires maximum number of transistors and maximum surface area among the three mentioned techniques. The STT requires number of transistors and surface area intermediate of the rest two techniques. It can be concluded that CMOS technique requires least number of transistors and consumes least area. However our aim is to design and analyse counter that consumes least power irrespective of how much area does it cover. Next, we measured power consumed by X-OR gate and 4-bit synchronous counter for different supply voltage in each technique.

TABLE IIIII: Total Power Dissipation by the Benchmark Circuits on 65nm Technology

Power Reduction Techniques	Benchmark Circuits					
	XOR Gate			1-Bit Adder		
	0.5 V	0.7V	0.9V	0.5 V	0.7V	0.9V
CCT	8.172	18.274	31.757	67.419	228	538
SST	0.234	0.465	0.861	37.89	125	291
FST	3.278	10.977	21.591	21.968	66.537	150

From the Table-III it can be observed that the power consumed by X-OR gate using CMOS technique is maximum and that by STT is minimum. We measured the power consumption on three different supply voltages i.e. 0.5 V, 0.7V and 0.9V.

TABLE IVV: POWER DIFFERENCE FOR X-OR GATE

Voltage (V)	% Difference in power b/w CMOS & STT	% Difference in power b/w CMOS & FST	% Difference in power b/w FST & STT
0.5	97.136	59.887	92.861
0.7	97.451	39.842	95.763
0.9	97.288	32.011	96.012
Average	97.291	43.91	94.878

TABLE V: POWER DIFFERENCE FOR 4-BIT SYNCHRONOUS COUNTER

Voltage(V)	% Difference in power b/w CMOS & STT	% Difference in power b/w CMOS & FST	% Difference in power b/w FST & STT
0.5	43.79	67.41	42.02
0.7	45.175	70.81	46.77
0.9	45.91	72.118	48.453
Average	44.958	70.112	45.747

The percentage difference in the power consumed is calculated using the formula

$$\%\text{Difference in power} = \frac{\text{Difference in Power}}{\text{Total Power}} \times 100$$

We calculated the percentage difference in power consumed by X-OR gate and that by counter using the above mentioned formula. The percentage differences in power consumed between every two techniques have been tabulated in Table-IV and Table-V.

VI. CONCLUSION

As counter is one of basic digital circuit of digital devices so power efficient counter design has become essential for the researchers. In this paper, we have designed a 4 - bit binary synchronous counter using CCT, STT and FST. The circuit designing and parametric analysis has been carried out using Microwind 3.1 and DSCH 3.1 designing tools. Various parameters have been observed on 65nm technology. From observations it can be concluded that the power consumed by FST counter and SST counter is much less as compared to power consumed by CMOS counter. The average power reduction was 44.9% in the case of SST and the average power reduction was 70.1% in the case of FST as compared to CMOS counter design. Although these techniques are power efficient as compared to CMOS technique but this is on the expense of larger surface area. Counter designed by these techniques can be useful where low power requirement will be primary concern.

REFERENCES

1. Yogita Hiremath, Akalpita L. Kulkurani, J.S. Baligar "Design and implementation of synchronous 4-bit up counter using 180nm CMOS technology," International Journal of Research in Engineering and Technology, Vol. 3, No.3, 2014.
2. Vinay Kumar Madasu, B Kedharnath "Leakage power reduction by using Sleep methods," International journal of engineering and computer science, Vol. 2, No.9, 2013.
3. Rajani H.P and Shrimannarayan Kulkarni "Novel Sleep transistor technique low leakage power peripheral circuits," International journal of VLSI design and communication system, Vol.3, No.4, 2012.
4. Kaushik Roy, Saibal Mukhopadhyay, Hamid Manmoodi-Meimand, "Leakage current mechanism and leakage reduction techniques in deep sub micrometer CMOS circuits," Proceedings of the IEEE, Vol.91, 2003.
5. Shilpa Shrigiri, Yogina Bellad "Low power VLSI design approach for 16 bit binary counter to reduce power," International journal of current engineering and technology.
6. Praween Sinha, Shreyaansh Shrivastava " Design of a low power 4 bit binary counter using Enhancement type MOSFET, International journal of research and technology Vol.1, No. 8, 2012.
7. Calvignac Yvan , Cambonie Pierre " 4-state binary counter; www.microwind.net
8. Sandeep Thakur, Rajesh Mehra, "Optimized Design and Simulation of Ring counter using 45nm technology," International journal of engineering trends and technology Vol. 36, 2016.