Design and VLSI Implementation of Low Voltage and Low Dropout Voltage Regulator

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ABSTRACT:

The usage of the battery power devices in today's global village has become pervasive and indispensable in almost every walk of life. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while minimizing quiescent current flow to increase battery life. An increasing number of low voltage applications require the use of LDOs, which include the growing family of portable battery products. Regulators are required to reduce the large voltage variations of the battery cells to lower and more acceptable levels. Absence of these power supplies can prove to be catastrophic in most high frequency and high performance circuit designs. As a result the demand for low-voltage, low drop-out regulators are increasing for portable electronics, such as, cellular phones, pagers and laptops. Here the project work deals with complete on-chip voltage regulator with improved transient response. Unlike the conventional LDOs, on-chip capacitance used in this design replaces the need for a large external capacitor allowing greater power system integration for SOC applications. Error amplifier was designed in order to meet high gain and the independent fast path circuit was employed to facilitate the LDO to respond quickly to the sudden load variations. This enabled reduction in the consequent ripple in the output voltage. The fast path was designed to enable easy migration to the other process without much degradation in the performance.

The designed LDO provides a constant voltage of 1.6V for a input voltage (Line Regulation) range of 1.8V to 3.3V, beyond which the pass transistor will be in triode region and it would not give a constant voltage of 1.6V. Load regulation was achieved at maximum voltage of 1.598V where the load resistance ($R_{L)}$ varied from 100Ω to 1kΩ. The LDO circuit was implemented in TSMC 0.18um CMOS technology. The Quiescent current of 25uA with a drop out voltage of 200mV was obtained. Maximum gain of 65dB and settling time of 6μsec was obtained due to the two stage op-amp and fast path circuit.

Key words: Low drop out, quiescent current, settling time, Line Regulation and Load Regulation

1. INTRODUCTION

The increases in demand for portable appliances emphasize the necessity of complete system-on-chip (SoC) design solutions with smaller sizes and lower operating voltages. The usage of the battery powered devices in today's global village has become pervasive and indispensable in

almost every walk of life. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while minimizing quiescent current flow to increase battery life. Current efficiency is particularly important because at low load current conditions and the life of the battery is adversely affected by low current efficiency or high current flow. In fact, the increasing drive towards total chip integration demands that power supply circuits be included in every chip.

In this low voltage environment, a low drop-out regulator is the most appropriate form of linear regulators. The low dropout voltage regulators have gained importance due to demand for power efficient circuits in mobile communications applications, which require increased battery life. While other classes of linear regulators provide better transient response and more load current, these low dropout regulators have the unique advantage of operating with very low ground currents and low input voltages.

Regulators are required to reduce the large voltage variations of battery cells to lower and more acceptable levels. Absence of these power supplies can prove to be catastrophic in most high frequency and high performance circuit designs. A series low dropout regulator is a circuit that provides a well specified and stable dc voltage whose input to output voltage difference is very low. The term series comes from the fact that a pass element is connected in series between the input and output terminals of the regulator. Low drop-out regulators can be categorized as either low power or high power, low power LDO's are those with a maximum output current of less than 1A, exhibited by most portable applications.

The operation of the LDO circuit is based on feeding back an amplified error signal to control the output current flow of the power transistor driving the load. In the design of LDO regulator, the main goal is to find the approach that allows one to avoid the on-chip compensating capacitors, which occupy a large chip area and to achieve the required stability using external off-chip load capacitance only. The LDO circuit becomes a single pole system with the pole defined by the gate capacitance of the pass transistor. The fast path circuit is introduced to reduce the settling time of the system.

Furthermore, most designs find it necessary to include regulators and other power supply circuits as products achieve or approach total chip integration. Low dropout regulators are appropriate for many circuit applications namely, automotive, portable, industrial and medical applications. In the automotive industry, the low dropout voltage is necessary during cold-crank conditions where the battery voltage can drop below 6V. Portable electronics market requires low voltage and low quiescent current flow for increased battery efficiency and longevity. As a result, high current efficiency is necessary to maximize battery life. Low voltage operation is also a consequence of the direction of process technology towards higher packing densities. In particular, isolation barriers decrease as the component densities per unit

area are increased thereby manifesting lower breakdown voltages.

The low dropout voltage regulator brings the advantage of power savings to system design by reducing the voltage required to maintain output regulation. Use of white-LED drivers has increased in recent years due to the popularity of colour LCD screens on most portable electronic equipment. The white backlight required to bring out the colour in these screens is most often provided by white LEDs. The lower forward voltage eliminates the need for voltage boosting, permitting the use of linear regulation topologies that reduce cost and solution size and increase efficiency across the battery discharge range. Finally, financial considerations also require that these circuits be fabricated in relatively simple processes, such as standard CMOS, bipolar and stripped down BiCMOS technologies.

The figure 1.1 illustrates the architecture of mobile phone power distribution system. The voltage supplied out of the battery varies between 3.0 V to 4.3 V, instead of being a constant voltage for corresponding units in the mobile phone. This gives rise to a situation where the entire system may get damaged. The LDO array utilized in the power distribution system correspondingly distributes the regulated voltages to the units.

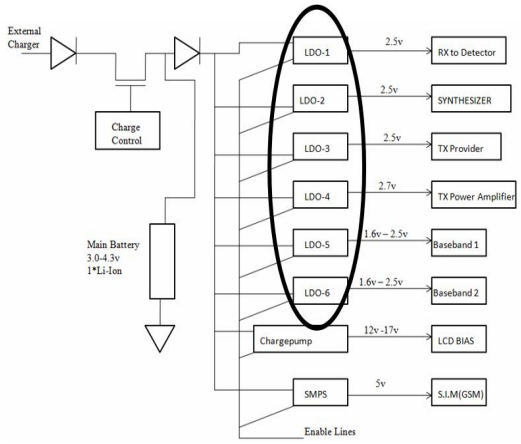

Figure 1 LDO in mobile power distribution [1]

2. PROBLEM DEFINITION

The objective of this project is to enhance performance of low drop-out regulators for battery powered electronics. This is targeted to fulfill the present commercial requirements as well as the projected demands of the future. The widespread use of battery-powered devices in today's world has increased the demand for low-voltage, low –dropout linear regulators (LDOs). The basic function of an LDO is to provide a reliable, constant output voltage to drive small sub-circuits, while extending battery-life in portable applications. The techniques that are developed to overcome the aforementioned obstacles not only enhance the prevailing LDO circuit architecture but also push regulator design into the twenty first century. This is carried out with existing standard technologies, thus the designs take full advantage of all physical aspects of the process while maintaining fabrication costs to acceptable and competitive levels. Moreover, the new design techniques will be able to further exploit the benefits of more advanced technologies in the future.

3. METHODOLOGY

Matthew Welborn [1] suggests that, to achieve data rates close 1.5 to 2 Gbps in 500 MHz bandwidth it would require scaling to 64-QAM, where there is a significant difference in power efficiency between QPSK and 64-QAM. For instance, the minimum Eb/N0 required at the receiver is 9.6 dB for BPSK at 10^{-5} bit-error rate (BER) and almost 10 dB higher for 64-QAM at the same BER. The result is that high order modulation requires higher transmit power in order to provide equivalent BER at the receiver. The tight constraints on UWB transmit power results in significant range performance differences in realistic operating conditions. The narrower bandwidth designs are extended to higher rates, the use of high order modulation and multiple antenna technologies can provide scalable and robust performance, but will also likely lead to increased complexity and power consumption. Systems that use wider bandwidths, such as direct sequence UWB, can use more efficient modulation and design approaches to provide wireless connectivity solutions that scale to even higher data rates with more scalable and lower complexity implementations.

The major drawback of Matthew Welborn [1] suggested architecture is the use single carrier systems against the multi carrier systems. The use of OFDM based systems results in efficient utilization of the spectrum, as compared to the single carrier systems. The use of multi carrier systems also increases the data rate with the low modulation schemes unlike the single carrier systems.

Oscar Robles Palacios and Carlos Silva Cardenas [5] suggest an architecture consisting of an oscillator based on direct digital synthesis (DDS) techniques, which is a digital control method of generating multiple frequencies from a reference clock signal [6]. This characteristic provides a system with great accuracy in terms of signal integrity. Thought the DDS and the IFFT functional units differ in many ways, it is important to mention that both of them will perform the same function, which is to transfer the signal from the frequency domain to the time domain. The ideal replacement of the IFFT functional unit in OFDM implementations is a DUC (Digital Up-Converter). Using DUCs is more suitable because they contain three filters (PFIR, CFIR and CIC) that accomplish a better spectral shaping of the signal. However, these filters increase the sample rate and delay, and required more synchronization hardware. The flexibility of the proposed design lies in the control unit of the system. The flexibility of this system lies in the Control Unit.This subsystem is in charge of analyzing the information inside the Instruction signal, and sending the appropriate orders to the rest of functional units. The four bits inside the instruction signal establish the constellation required for each subcarrier. Hence, the Control Unit must send 2-bit word to appropriate I&Q Mapper. The system is thus capable of performing a different modulation technique for each

subcarrier. The architecture of the implemented NCO shows the simplicity and flexibility of the subsystems. The main functional unit of this subsystem is the Phase Accumulator. This stage receives the clock and the TWN -Tuning Word assigned to the N sub-channel signals and goes through the entire count.

The major drawback of the Oscar Robles Palacios and Carlos Silva Cardenas [5] is the use of NCO rather than the use of DUC, albeit increase in system latency and need of synchronization hardware.

4. DESIGN AND IMPLEMENTATION

4.1 Design Specification

There are many reference topologies available for a variety of different applications and process technologies. Currently, a large portion of the market demand is driven by portable electronic products whose operating voltages range from 0.9V to 5V.

Table 1 Design specifications of the system

Description	Specification
Technology	TSMC 180nm CMOS Process
Input Voltage (V_{in})	1.8V to 3.3V
Voltage Reference (V_{ref})	1.2V
System Gain	50dB-70dB
Output Voltage (V_{out})	1.6V
Temperature	-20^0C to 80^0C
Quiescent Current	<50 µA
Vdrop-out	<300mV

The input voltage to the system is fed within the range of 1.8V to 3.3V. The reference voltage for the system is 1.2V. The output voltage of the system is a constant 1.6V. The gain of the system is 65dB. The operating temperature of the system is within the range -20^0 C to 80^0C. The quiescent current of the system is lesser than 50 micro amperes. The system with a quiescent current greater than 50 micro amperes leads to higher power consumption. The chip area of the LDO is $0.1mm^2$.

4.2 Design of Error amplifier

The error amplifier consists of a pair of load transistors, a pair of differential transistors and a tail transistor as shown in figure 6.1. The active load acts as a current source. It must be biased such that their current adds up exactly to I_{ss}. The current mirror consists of transistors M3 and M4. One transistor M3 is always connected as a diode and drives the other transistor M4. Since $V_{gs3} = V_{gs4}$, and if both the transistors have same beta, then current through M3 and M4 are I_{d3} and I_{d4} (i.e. $I_{d3} = I_{d4}$). The advantage of this configuration is that the differential input is converted to a single ended output signal

with no extra component required. One input for the differential amplifier will come from the feedback resistor and second input is directly taken from voltage reference circuit. In error amplifier circuit the output voltage or current is taken from the drains of M2 and M4. The output coming from these two will drive the pass transistor. Under quiescent conditions the two currents in transistors M1 and M2 are equal.

The current that is flowing in M1 will be same as in M3 and is mirrored to M4. If V_{gs2} = V_{gs2} and M1 and M2 should be equal to the current that M2 requires, causing I_{out} to be zero provided that the load is negligible. In above analysis it is necessary to keep every transistor is in saturation region. If $V_{gs1} > V_{gs2}$ then, I_{d1} increases with respect to I_{d2} since $I_{ss} = I_{d1} + I_{d2}$. This increase in I_{d1} implies an increase in I_{d3} and I_{d4}. However, I_{d2} decreases when $V_{gs1} > V_{gs2}$. Therefore, the only way to establish circuit equilibrium is for I_{out} to become positive and V_{out} to increase. It can be inferred that when $V_{gs1} < V_{gs2}$ then I_{out} becomes negative and V_{out} decreases.

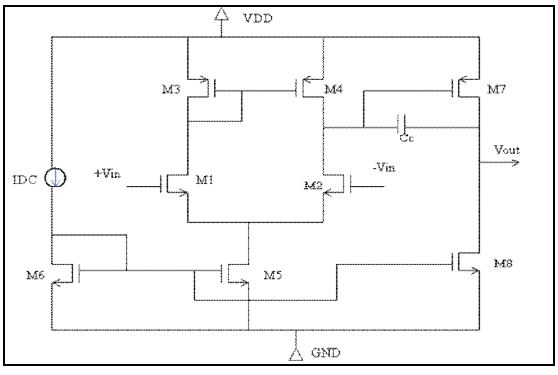

Figure 2 Error amplifier architecture

4.3 Design of 16-QAM

The dropout voltage of the proposed LDO was selected to be 200mV for a maximum load current of 50mA based on current LDO regulatory requirements. In device parameters, the pass transistor is designed to deliver a drain current of 50mA while maintaining a saturation voltage, $V_{DS} > V_{GS} – V_T$, of 200 mV. The W/L ratio has to be maintained as high as possible for the pass transistor to improve PSRR and slew rate. The pass element is employed in common source configuration as against the common drain in the case of conventional voltage regulators. Improved efficiency relative to the conventional regulators is achieved by replacing the common-drain pass element with a common-source one to reduce the minimum required voltage drop across the control device. The consequence of low voltage drop across the pass element is that the overall power dissipation is reduced. This facilitates the design of a low voltage, on chip regulator.

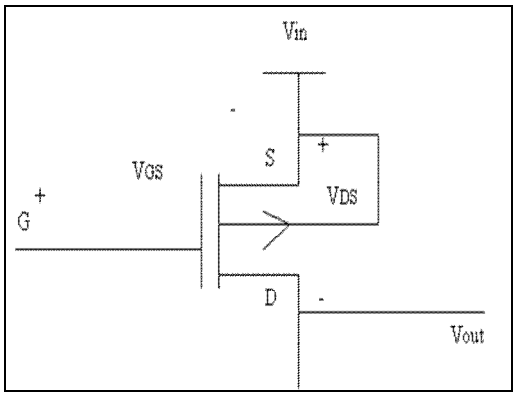

Figure 3 Pass Transistor

4.4 Design of feedback network

The feedback network is nothing but a voltage divider which is giving a portion of the output voltage of the LDO as feedback voltage to the input of the error amplifier for the comparison and making a stable output voltage. The feedback network is formed by using two resistors R1 and R2. Here the resistors are chosen by using the voltage divider formula for getting an output voltage of 1.6V and the non-inverting input voltage of 1.2V. The figure 6.3 illustrates the feedback network utilized in the design of LDO.

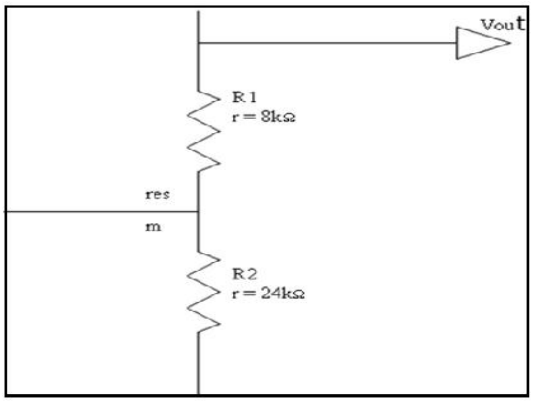

Figure 4 Feedback network

4.4 Design of feedback network

To provide a qualitative understanding of the circuit behaviour, the circuit can be analyzed using a simple square law MOS model. The operation as follows; transistors T2, T3 and T4 are saturated and T1 works in the triode region. The effect of supply-voltage variations is twofold. Suppose V_{DD} increases. First, since the currents of T1 and T2 are the same, the gate-source voltage of T1 will increase proportional to the increase in V_{DD}. Therefore the voltage V_2 will also increase proportionally. Secondly, the gate-source voltage of T3 increases with V_{DD} due to its gate is connected to V_2. Therefore, despite the body effect, its drain current will increase proportionally with the increase in V_{DD}. The circuit is designed so that the required increase in current through T3 is provided by the increase in T4´s current.

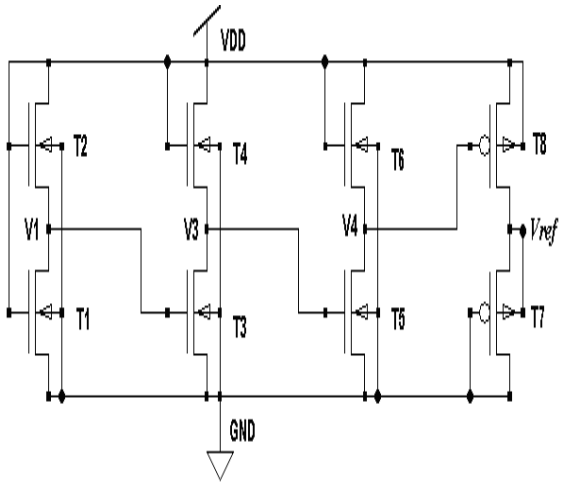

Figure 5 Voltage reference circuit

As a result V_3 will remain constant with changing V_{DD}. Transistors T5 and T6 (both are saturated) have to convert from a supply-independent threshold-referenced NMOS voltage (V_3) relative to ground to a voltage relative to V_{DD}. The final result is that V_{DD}–V_4 will remain constant with changing V_{DD} for a given range of values. Transistor T7 and T8 will act as a subtractor of both V_{THN} and V_{THP} which have different weighting factors to form a reference voltage.

5 VALIDATIONS AND DISCUSSION OF RESULTS

The table 2 displays the resource utilization summary and the corresponding achieved results of low dropout (LDO) voltage regulator after the simulation process targeted for virtuoso schematic editor tool. The tabulated results clearly indicate that LDO results in lesser resource utilization with minimum dropout, lower quiescent current at higher load conditions. The system gain is high, it indicates the stability of the system is good.

Table 2 Summary of Measured Performance of LDO

Description	**Specification**	**Achieve Parameters**
Technology	TSMC 180nm CMOS Process	TSMC 180nm CMOS Process
Input Voltage (V_{in})	1.8V to 3.3V	1.8V to 3.3V
Voltage Reference (V_{ref})	1.2V	1.2V
System Gain	50dB-70dB	65dB
Output Voltage (V_{out})	1.6V	1.6V
Temperature	-20^0C to 80^0C	-20^0C to 80^0C
Quiescent Current	<50 µA	25µA
Vdrop-out	<300mV	200mV

Dropout is the minimum input – to – output differential voltage at which the circuit ceases to regulate against further reductions in input voltage. The worst case dropout voltage achieved in the design is of 200mV. The input voltage is varied from 1.8V to 3.3V and regulated output of 1.6V was obtained. The reference voltage of 1.2V was provided at the inverting terminal of the op-amp, and same reference voltage was maintained at non-inverting terminal. For maintaining 1.2V at non-inverting terminal resistor values as R1 = 8kΩ and R2 = 24kΩ were utilized. Voltage divider formulae were used to obtain the resistor values.

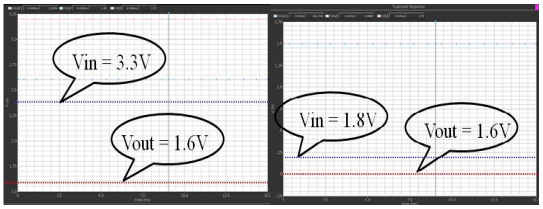

Figure 6 Transient response of LDO

Load regulation performance is enhanced as the open-loop gain of the system is increased. However the gain is limited by the unity gain frequency, therefore care must be taken to design the unity gain frequency of the amplifier.

The unity gain frequency of the amplifier decides the settling time during the transient response. In order to achieve a load regulation of .01%, the error amplifier gain

should be as high as 60-70dB. Pass transistor provides approximately 10dB gain. Hence the requisite gain for the error amplifier is 60dB. A gain of 65dB was achieved.

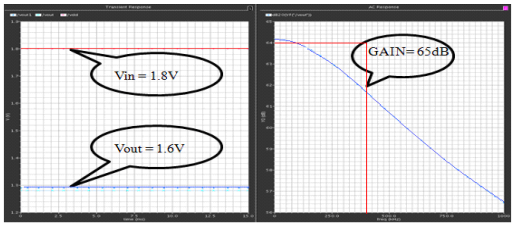

Figure 8 Specifications and Simulation results of LDO in VSE

The placement of the blocks of LDO is such that the layout of the design occupies minimum amount of area and with good matching. The input and output blocks are critical hence must be protected using guard ring. Careful matching was also used in between the two feedback resistors R1 and R2 by interleaving unit resistors to meet the desired ratio.

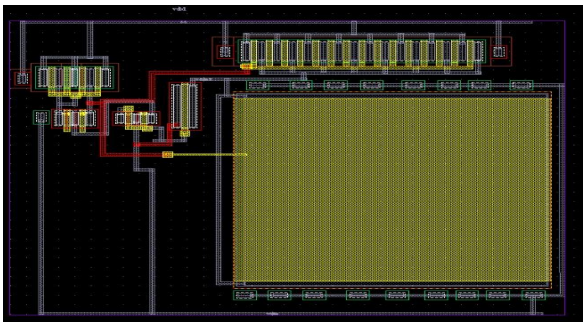

Figure 7 Layout design of LDO regulator

It is extremely important that the layout design must not violate any of the Layout design rules of the fabrication process, in order to ensure a high probability of defect-free fabrication of all features described in the mask layout.

6 CONCLUSIONS

- The LDO design flow carried out in H-spice and circuit level implementation has been carried out in Cadence Schematic, Editor Layouts for the complete LDO design have been carried out in Cadence Layout XL, using diffusion sharing technique.
- The designed LDO provides a constant voltage of 1.6V for a input voltage (Line Regulation) range of 1.8 V to 3.3 V, beyond which the pass transistor goes in to triode region and it would not give a constant voltage of 1.6 V
- Load regulation was achieved at maximum voltage of 1.598 V where the load resistance ($R_{L)}$ varied from 100 Ω to 1 kΩ. The LDO circuit was implemented in TSMC 0.18 µm CMOS technology
- The Quiescent current of 25 µA with a drop out voltage of 200 mV was obtained. Maximum gain of 65 dB and settling time of 6µsec was obtained with the help of two stage op-amp and fast path circuit

7 RECOMMENDATIONS FOR FUTURE WORK

- The LDO design can be targeted for low load conditions and the input range can be widened with the help of design modifications
- The LDO design with different circuit topologies can further decrease dropout voltage by 200 mV

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