Power Reduction and Speed Augmentation in LFSR for Improved Sequence Generation Using Transistor Stacking Method

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***Abstract*-In many electronics circuit Linear Feedback Shift Register (LFSR) used for generating sequences. So for high performance applications LFSR should have to generate efficient sequences. There are so many methods of generating very efficient sequences. The demand and popularity of portable LFSR is driving designers to strive for small silicon area, higher speeds, low power dissipation and reliability. Compared to static LFSR, dynamic LFSR offers good performance. Wide fan-in logic such as domino LFSR is used in high-performance applications. Dynamic domino LFSRs are widely used in modern digital VLSI circuits. These dynamic LFSRs are often favored in high performance designs because of the speed advantage offered over static LFSR circuits. This paper compares different types of LFSR on the basis of performance parameter such as power consumption, propagation delay and leakage current at 65 nm, 45 nm, 32 nm and 25nm technologies for high performance LFSR design. The techniques are compared by performing detailed transistor simulations on benchmark circuits using Microwind 3 and DSCH 3 CMOS layout CAD tools.**

***Key words*- LFSR, Leakage current, Power dissipation, Propagation Delay and VLSI.**

I. Introduction

An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops. The aim of this paper is to compares static LFSR, domino (dynamic) LFSR and different types of LFSR which are designed by different components (Transmission gates and inverter, Pass transistors) on the basis of performance parameter such as power consumption, delay, power delay product, no of transistors use and leakage current at 65 nm, 45 nm, 32 nm and 25nm technologies.

II. Power Dissipation

The power consumed by CMOS circuits can be classified into two categories:

A. Dynamic Power Dissipation

For a fraction of an instant during the operation of a circuit, both the PMOS and NMOS devices are “on” simultaneously. The duration of the interval depends on the input and output transition (rise and fall) times. During this time, a path exists between VDD and GND and a short-circuit current flows. However, this is not the dominant factor in dynamic power dissipation. The major component of dynamic power dissipation arises from transient switching behaviour of the nodes. Signals in CMOS devices transition back and forth between the two logic levels, resulting in the charging and discharging of parasitic capacitances in the circuit. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation. [15]

B. Static Power Dissipation

This is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The sub threshold leakage current increases exponentially, thereby increasing static power dissipation. [15]

- Formula for Power Dissipation:

$P_d = (I_{avg}) \times (V_{dd})$ [16]

Where, I_{avg} = average current,

V_{dd} = applied voltage.

- Formula for Leakage Current:

$I_{leakage} = I_0 \exp(v_{gs}-v_{th})/n\, v_t$ [17]

Here,

$I_0 = \mu_0 C_{ox}[W/L]V_t\, 2\, e^{1.8}$

- Formula for Propagation delay:

$T_{pd} \alpha (V_{dd}/(V_{dd}-V_{th})^2)$ [18]

Where,

C_{ox}= Gate oxide capacitance,

(W/L) = Width to length ratio of the leaking MOS device,

μ_0 = Zero bias mobility,

V_{gs} = Gate to source voltage,

V_t = Thermal voltage and

n=2 (Sub-threshold swing coefficient)

T_{pd}= Propagation delay

V_{dd} = Supply Voltage

V_{th} = Threshold Voltage

III. Problem Identification

For driving the MOSFET (Metal Oxide Semiconductor Field effect transistor) key parameter is the scaling of the transistor gate length, which has a significant performance impact at the 32nm node & beyond. Because of the large gate tunnelling currents, the gate oxide cannot be further scaled down and beyond the 45nm node the channel length scaling without gate dielectric scaling actually degrades transistor drive current and performance. For further reduction in scaling technology beyond the 45nm node the high-k dielectric material is introduced as gate dielectric layer. As the gate oxide thickness of a transistor reduces, performance of the transistor become poor. This will give the negative impact on all over performance of the CMOS logic circuit. For achieving this purpose semiconductor engineers have continuously decreases the thickness of the gate dielectric layer, higher leakage current will be resulted in the reduced dielectric thickness.

Leakage power has become a serious concern in nanometer CMOS technologies. In the past, the dynamic power has dominated the total power dissipation of CMOS devices. However, with the continuous trend of technology scaling, leakage power is becoming a main contributor to power consumption.

IV. Proposed Methodology

A. *Using Transistor Stack*

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the "Stacking Effect" [21].When two or more transistors that are switched OFF are stacked on top of each other [Refer Fig.1], and then they dissipate less leakage power than a single transistor that is turned OFF [Refer Fig.1]. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage. Therefore in Fig.10a transistor T_2 leaks less current than transistor T1 and T_3 leaks less than T_2. Hence the total leakage current through the transistors T_1, T_2 and T_3 is decreased as it flows from V_{dd} to Gnd. So I_{leak1} is less than I_{leak2}. If natural stacking of transistors does not exist in a circuit, then to utilize the stacking effect a single transistor of width W is replaced by two transistors each of width W/2. The proposed D flip-flop circuit using stacking effect is shown in Fig.2. The leakage reduction achievable in a two-stack comprising of devices with widths Wu and W_l compared to a single device of width w is given by equation 5. [22]

$$X = \frac{I_{device}}{I_{stack}} = \frac{w}{w_u^{\propto} w_l^{1-\propto}} 10^{\frac{\lambda_d V_{dd}}{s}(1-\propto)} \quad \ldots.(1)$$

Where $\propto = \frac{\lambda_d}{1+2\lambda_d}$ ….(2)

$\lambda_d$is the drain-induced barrier lowering (DIBL) factor and s is the sub-threshold swing coefficient.

When $w_u = w_l = w/2$ then the leakage reduction factor or stack effect factor X is rewritten as

$$X = \frac{w}{\frac{w^{\propto}}{2}\frac{w^{1-\propto}}{2}} 10^{\frac{\lambda_d V_{dd}}{s}(1-\propto)} \quad \ldots.(3)$$

$$X = 2 \times 10^{\frac{\lambda_d V_{dd}}{s}\left(\frac{1+\lambda_d}{1+2\lambda_d}\right)} \quad \ldots.(4)$$

$$X = 2 \times 10^{u} \quad \ldots.(5)$$

Where u is the universal two-stack exponent which depends only on the process parameter, $\lambda_d$and s, and the design parameter V_{dd}. Thus the leakage current through a single OFF device is greater than leakage through a stack of two OFF devices.

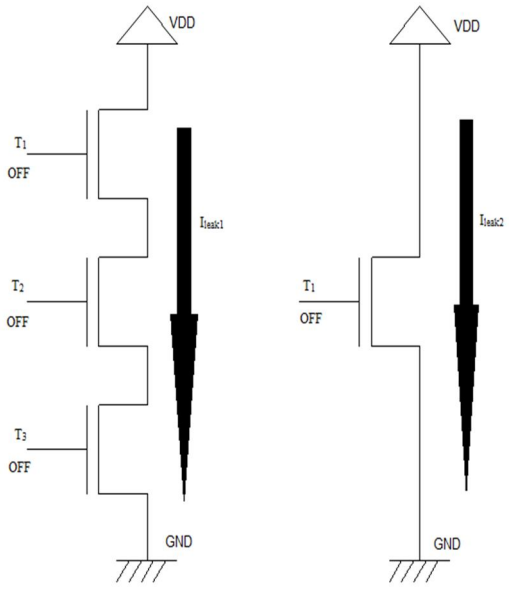

Fig.1. Transistor stacking effect [21]

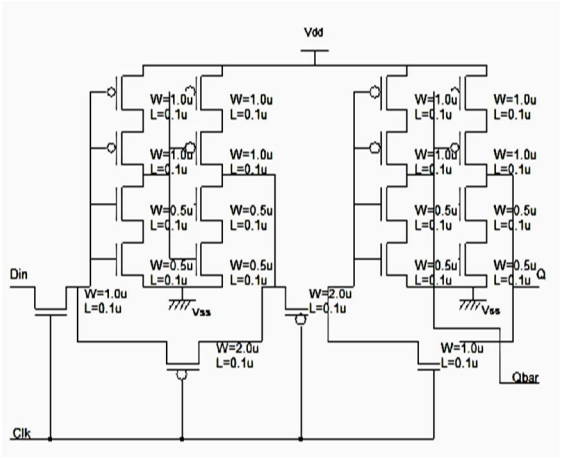

Fig.2. D flip-flop with transistor stacking [21]

Here four types of circuits are used which are given below.

1) Static Logic Circuit

The principle of static CMOS logic is shown in Fig.3 the output is connected to ground through an n-block and to V_{DD} through a dual p-block. Without changes of the inputs this gate consumes only the leakage currents of some transistors. When it is switching it draws an additional current which is needed to charge and discharge the internal capacitances and the load. Although the gate's logic function is ideally independent of the transistor channel widths, they determine the dynamic behaviour essentially.

Wider transistors will switch a capacitive load faster, but they will also cause a larger input capacitance of the gate. Unless otherwise noted, minimum-width and, of course, minimum-channel-length transistors are assumed. For given capacitances the transistors' on-state current I_{ON} will limit the switching speed of the gate and, consequently, the maximum clock frequency of a synchronous circuit. Two other important parameters determining the speed are the so-called fan-in F_{in} which is the number of inputs of a gate, and the fan-out V_{out} which is the number of unity loads (i.e., inputs) connected to a gate's output [19].

Advantages of Static Logic Circuits

- High noise margins.
- Low output impedance, high input impedance.
- No steady state path between V_{DD} and GND (no static power consumption).
- Delay a function of load capacitance and transistor resistance comparable rise and fall times (under the appropriate transistor sizing conditions).

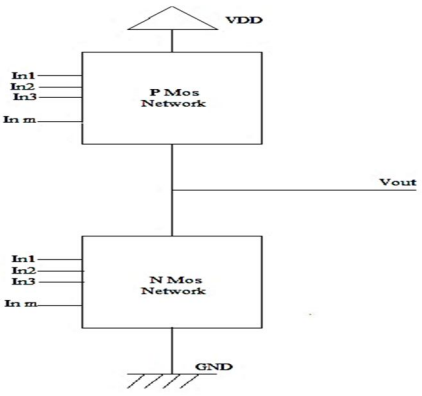

Figure 3. Static Logic Circuit [19]

2) Dynamic Logic Circuit

Dynamic logic circuits offer several advantages in realizing high-density, high performance digital system where reduction of circuit delay and silicon area is important. Operation of all dynamic logic gates depend on temporary storage of charge in parasitic node capacitances, instead of relying on steady-state circuit behavior. Dynamic logic circuits require periodic clock signals in order to control charge refreshing.

Dynamic logic techniques save area by reducing the number of transistors per gate, and save power by reducing the number of gates and the static current in structures such as flip-flops & shift registers. Dynamic CMOS circuits save chip area while enhancing speed over conventional CMOS circuits, but precautions must be taken to ensure proper operation.

Use of common clock signals the system enables synchronize the operation of various circuit blocks. Capability of temporarily storing a state at a capacitive node allows implementing simple sequential circuits with memory functions.

Disadvantage of dynamic storage is the use of small-sized, leaky capacitors for storing logic values. They must be clocked at a minimum operating frequency in order to maintain their charge.

In Dynamic CMOS logic, I_{DD} Path is turned off when clock-disabled and/or the output is evaluated when clock enabled. Circuit operation is based on first pre-charging the output node capacitance and evaluating the output level according to the applied inputs as shown in figure 4. Both operations are scheduled by a single clock signal which drives one nMOS and one pMOS transistor in each dynamic stage.

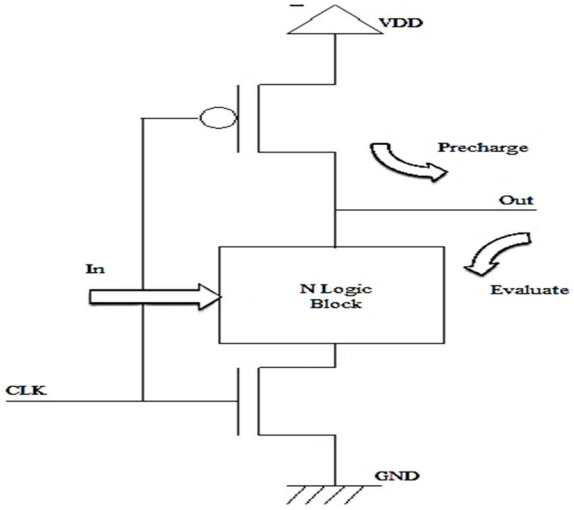

Figure 4. Dynamic Logic Circuit [19]

3) Pass Transistor Logic Circuit

The pass transistor, MP is driven by periodic clock signal and acts as access switch to either to charge up or down the parasitic capacitance C_x, depending on V_{in}. Two operations are possible when CK = 1. Logic '1' transfer and logic '0' transfer. The output of depletion-load nMOS inverter depends on voltage V_x. MP provides only current path to the intermediate capacitive node (soft node) X. When CK = 0, the MP ceases to conduct and charge stored in the parasitic capacitor C_x continues to determine output level of the inverter.

i. Logic '1' Transfer

If the soft node voltage is equal to 0 initially, i.e., $V_x(t = 0) = 0$ V. Logic '1' level is applied to the input terminal, which corresponds to $V_{in} = V_{DD}$. When CK changes from 0 to 1, MP

will be in saturation. The equivalent circuit for logic '1' transfer is shown in figure 5.

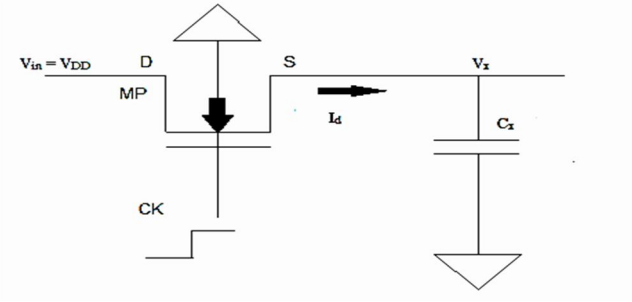

Figure 5. Equivalent circuit for logic '1' transfer

The pass transistor MP operating in the saturation region starts to charge up the capacitor C_x, since, I = C dV/dt. Thus,

$$C_x \frac{dV_x}{dt} = \frac{k_n}{2}(V_{DD} - V_x - V_{T,n})^2$$

Then Vx(t) is

$$V_x(t) = \frac{\frac{k_n}{2C_x}(V_{DD} - V_{T,MP})t}{1 + \left(\frac{k_n}{2C_x}(V_{DD} - V_{T,MP})\right)t}(V_{DD} - V_{T,MP})$$

Variation of node voltage V_x w.r.t. last equation is plotted as a function of time is shown in figure 6.

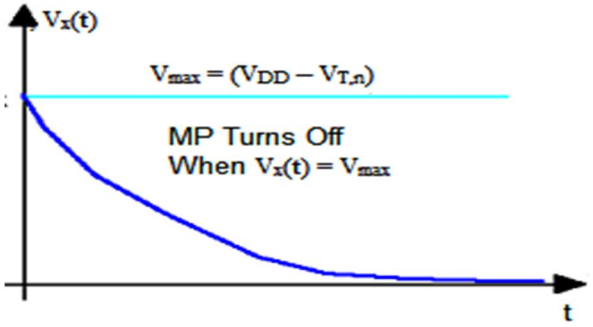

Figure 6. Variation of node voltage as a function of time during logic '1' transfer

ii. Logic '0' Transfer

If the that soft node voltage is equal to 1 initially, i.e., $V_x(t = 0) = V_{max} = (V_{DD} - V_{T,n})$. Logic '0' level is applied to the input terminal, which corresponds to V_{in} = 0 V. When CK changes from 0 to 1, MP will be in linear region. The equivalent circuit for logic '0' transfer is shown in figure 7.

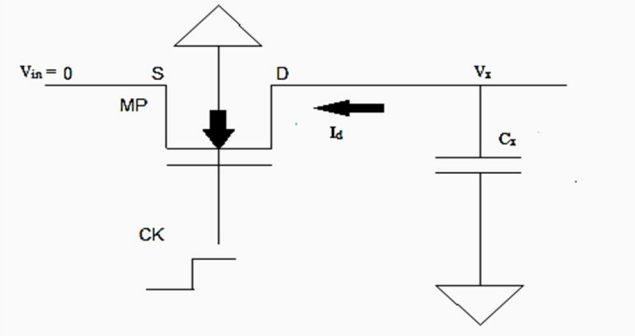

Figure 7. Equivalent circuit for logic '0' transfer

The direction of current flow through will be opposite to that during charge-up event. The pass transistor MP operating in the linear region discharges the parasitic capacitor C_x as follows:

$$-C_x \frac{dV_x}{dt} = \frac{k_n}{2}(2(V_{DD} - V_{T,n})V_x - V_x^2)$$

Integrating above equation w.r.t. t we get,

t =

$$\frac{C_x}{k_n(V_{DD} - V_{T,n})} \ln\left(\frac{2(V_{DD} - V_{T,n}) - V_x}{V_x}\right)$$

Variation of node voltage V_x w.r.t. last equation is plotted as function of time is shown in figure 8.

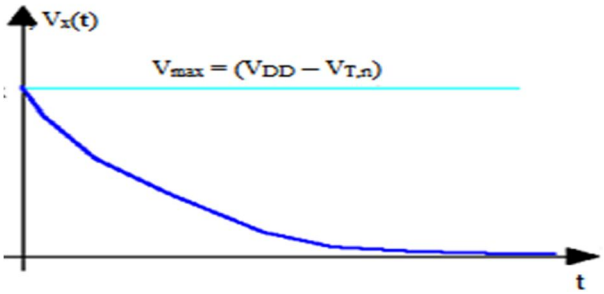

Figure 8. Variation of node voltage as a function of time during logic '0' transfer.

Fall time for the soft node voltage V_x can be calculated from previous equation.

$$\tau_{fall} = 2.74\frac{C_x}{k_n(V_{DD} - V_{T,n})}$$

Advantages of pass transistors are:

- They are not ratio devices and can be minimum geometry.
- They do not have a path from plus supply to ground, do not dissipate standby power.
- They are used as function block.
- Very efficient in use of transistor.
- Potentially very efficient layouts results.
- Pass transistors can usually be minimum size devices. Usually more internal node capacitance than with conventional CMOS gates.
- Propagation delays can become large in long series strings of pass transistors.
- Static power dissipation is unaffected.
- Dynamic power dissipation may be decreased.

The disadvantage of pass transistor logic circuit is that if the threshold voltages of all transistors are same, then the node voltage at the end of the pass transistor chain will become one threshold voltage lower than V_{DD}, regardless of number of pass transistors in chain. [19]

4) Transmission Gate Logic Circuit

CMOS TG consists of one nMOS and one pMOS transistor connected in parallel is shown in figure 9. CMOS TG operates as a bidirectional switch between the nodes A and B which is controlled by signal C. If C is high, both the transistors are turned on and provide a low resistance current path between the nodes A & B. If C is low, both the transistors are turned off and path between the nodes A & B will be an open circuit, called high-impedance state.

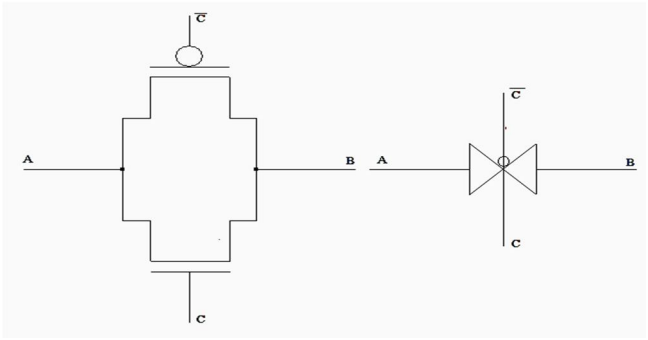

Figure 9. CMOS Transmission Gate [19]

A CMOS transmission gate can be constructed by parallel combination of NMOS and PMOS transistors, with complementary gate signals.
The main advantage of the CMOS transmission gate compared to NMOS, transmission gate is to allow the input signal to be transmitted to the output without the threshold voltage attenuation.

V. Output

In this paper CMOS implementations of LFSRs using static logic circuit, dynamic logic circuit, pass transistor logic circuit, and transmission gate logic circuit are designed. This LFSR design using pass transistor logic has the maximum delay, minimum average power and use maximum number of transistors. The leakage power and leakage current of all the designs are decrease when reduction techniques are applied. The percentage reduction of leakage power is more with the proposed transistor stacking technique. The design using Transmission gate logic circuit and Dynamic logic are given least delay and Dynamic logic circuit is use less number of transistors then others. The design of LFSR using pass transistors with transistor stacking technique is give the minimum leakage power and leakage current. But, if the threshold voltages of all transistors are same, then the node voltage at the end of the pass transistor chain is become one threshold voltage lower than VDD, regardless of number of pass transistors in chain. So that due to this disadvantage of pass transistor we use dynamic logic circuit with transistor stacking for designing high performance LFSR.

Table. 1. Power Dissipation

SCALE	Static Logic Ckt	Static Logic Ckt with Transistor Stacking	Domino Logic Ckt	Domino Logic Ckt with Transistor Stacking
65nm	0.302mW	0.324mW	33.87 µW	14.155 µW
45 nm	33.311 µW	33.590 µW	5.317 µW	3.399 µW
32 nm	20.681 µW	21.093 µW	3.737 µW	2.330 µW
25 nm	6.047mW	5.164 mW	1.73 mW	0.865 mW

Table. 2. Power Dissipation

SCALE	Pass Transistor Logic Ckt	Pass Transistor Ckt with Transistor Stacking	Transmission Gate and Inverter Logic Ckt	TG and I Logic Ckt with Transistor Stacking
65nm	15.35 µW	8.41 µW	23.787 µW	17.528 µW
45 nm	4.452 µW	2.336 µW	11.65 µW	9.150 µW
32 nm	3.662 µW	1.889 µW	7.274 µW	5.70 µW
25 nm	0.695 mW	0.41 mW	1.537 mW	1.175 mW

Table. 3. Leakage Current

SCALE	Static Logic Ckt	Static Logic Ckt with Transistor Stacking	Domino Logic Ckt	Domino Logic Ckt with Transistor Stacking
65nm	0.431mA	0.46 mA	0.048mA	0.02 mA
45 nm	0.083mA	0.084mA	0.013mA	0.008mA
32 nm	0.059mA	0.060mA	0.011mA	0.007mA
25 nm	2.419mA	2.065mA	0.709mA	0.864mA

Table. 4. Leakage Current

SCALE	Pass Transistor Logic Ckt	Pass Transistor Ckt with Transistor Stacking	Transmission Gate and Inverter Logic Ckt	TG and I Logic Ckt with Transistor Stacking
65nm	0.022 mA	0.012mA	0.034mA	0.025mA
45 nm	0.011mA	0.006mA	0.029mA	0.023mA
32 nm	0.010mA	0.005mA	0.021mA	0.016mA
25 nm	0.278mA	0.164mA	0.615mA	0.47 mA

Table. 5. Propagation Delay in 32 nm

SCALE	Static Logic Ckt	Static Logic Ckt with Transistor Stacking	Domino Logic Ckt	Domino Logic Ckt with Transistor Stacking
32 nm	16ps	42ps	16ps	20ps

Table. 6. Propagation Delay in 32 nm

SCALE	Pass Transistor Logic Ckt	Pass Transistor Ckt with Transistor Stacking	Transmission Gate and Inverter Logic Ckt	TG and I Logic Ckt with Transistor Stacking
32 nm	38ps	42ps	17ps	25ps

Table. 7. No. of Transistors

Static Logic Ckt	Static Logic Ckt with Transistor Stacking	Domino Logic Ckt	Domino Logic Ckt with Transistor Stacking
45	90	44	88

Table. 8. No. of Transistors

Pass Transistor Logic Ckt	Pass Transistor Ckt with Transistor Stacking	Transmission Gate and Inverter Logic Ckt	TG and I Logic Ckt with Transistor Stacking
60	120	56	112

VI. Application

The application of LFSRs are given below

- Pseudo-noise sequences
- Fast digital counters
- Whitening sequences
- Pattern Generators
- Built-in Self-Test (BIST)
- Encryption
- Compression
- Checksums
- Pseudo-Random Bit Sequences (PRBS)

VII. Conclusion

On the basis of the whole performance the Pass transistor logic has minimum power dissipation and leakage current but it cannot be cascaded with each other so that domino/dynamic logic is used for designing high performance LFSR.

From the whole system design and performance analysis it can be easy to conclude that system designed on 32nm scale will always give very high performance in comparison to other.

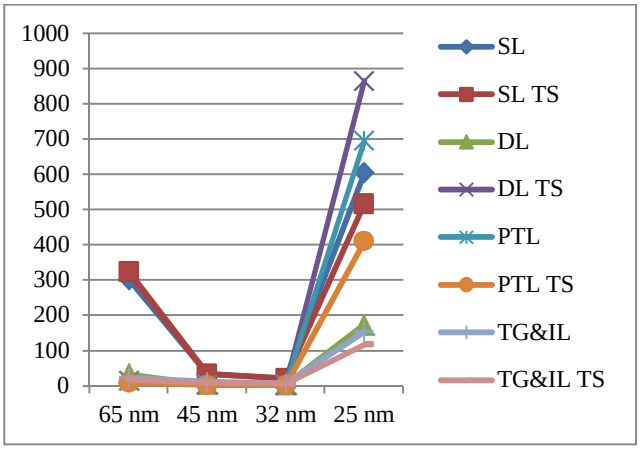

Figure 10. Power Dissipation (Micro Watt) in Different Technology

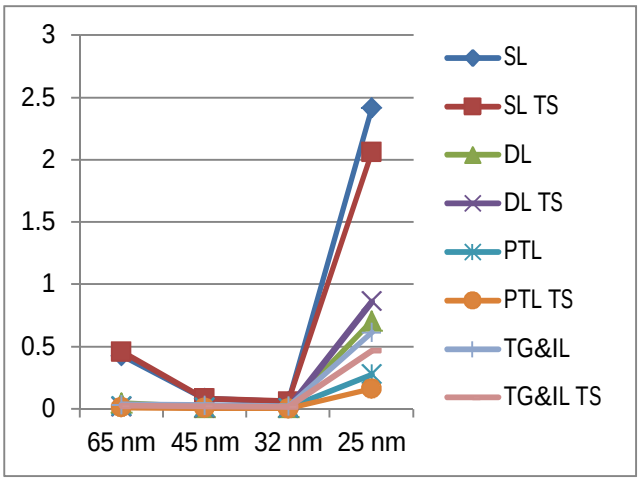

Figure 11. Leakage Current (mA) in Different Technology

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