# An Optimal Swarm Intelligence Approach For Test Sequence Restructuring To Conserve Power Usage In VLSI Testing

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**Abstract: Energy dissipation during testing has been discovered to be more than during regular mode due to increased switching activity. Test Sequence restructuring approach helps mitigate this problem as it allows the decrease of switching action during testing. This research presents a new Test Sequence restructuring approach. A cross model of genetic and pharaonis algorithms devised to restructure the test sequence. The model devised here is empirically verified with ISCAS'85 standard circuits that evident the minimization of switching activity to approximately to 32%.**

*Keywords:VLSI testing, swarm intelligence Testing, Test Sequence Restructuring,*

## INTRODUCTION

For CMOS circuits, there are only two principal sources of energy dissipation: dynamic dissipation as a result of discharging of load capacitances and changing transient current and static debauchery due to leakage current through the conduit and the channeling current through the gate oxide determined. For existing CMOS technology, dynamic dissipation may be the dominant source of power dissipation and it is proportional to the number of changing action within the circuit. Changing activity in a signal might be a lot better during test than during normal operation. It is because serial practical input vectors placed on a given circuit during program mode have a significant correlation and in scenario, the extra energy consumption might ruin circuits [22].

Several techniques are suggested to deal with the problem of decrease test energy. Authors in [17] used low loss blocking routine together with non-critical inputs simply. Key drawbacks of the strategy include region and practical timing overheads and check enable link timing closure. Another strategy is to split the scan chain into several scan sections [20]. Scan chain modification is a system that targets at subordinating the number of transitions in scan chain during change period. Re-ordering of scan chain may divergence with other objectives throughout scan chain optimization together with timing closure and line length minimization. The easiest strategy to make the transition throughout test similar to that of the normal function will be to re-order the Test Sequence which decreases the internal switching action by reducing transition density at signal inputs [12][3][8]. Altering the order of application Test Sequence from consumed to signal under test can reduce test power. The techniques apply basting detachment to the restructuring of Test Sequences [1] [14]

For this specific purpose, the proposed technique reduces the complete switching activity by decreasing the switching activity at circuit inputs. The object is to find an ideal Test Sequence ordering for a specified tests succession such that the switching movement in the circuits is smallest amount. In this system for Test Sequence order, Test Sequences are like towns as well as their Hamming distance are distance between cities. This algorithm combines genetic algorithm together with the better crossover machinist and mutation operator which makes the confined optimal solution cross and transform, then enhances the algorithm's search and improves the capability to find feasible solutions. The strategy regards as combinational circuits or full scan in order circuits and has no consequence in the first flaw coverage. Compared with existing Test Sequence ordering strategies, this method is easily the most effective alternative proposed up to today. This characteristic is illustrated with the results collected in the benchmarks.

## ASSOCIATED WORK

The two mechanisms of power dissipated in a CMOS circuit are static dissipation ( $P_{st}$ ) and dynamic debauchery due to switching passing current ( $P_{sc}$ ) and discharging of load capacitances ( $P_d$ ). The total power dissipation ( $P_{total}$ ) is given by:

$$P_{total} = P_{st} + P_{sc} + P_d \quad (1)$$

In above three parts, $P_d$ is the main source of power dissipation. $P_d$ can be considered using the subsequent equation:

$$P_d = \frac{1}{2}\alpha C V_{dd}^2 f \quad (2)$$

where, $V_{DD}$ and C are the power supply voltage and the entire capacitance of circuit, correspondingly. These values depend on the selected technology and cannot be attuned in the design phase. F is the clock frequency and is determined based on the normal process of circuit slightly than the test mode. $\alpha$ Is the incidence probability of a transition.

To decrease power expenditure in the design phase, the frequent way is to decrease the switching activity since this factor completely depends on the propose and test policy. Therefore, the aim is to find out the finest order of Test Sequence application to minimize power indulgence. The test set restructuring can be concentrated to the well-known peripatetic salesman problem [18][5][11][19] where the personage Test Sequences are the cities and the Hamming distance among any two Test Sequences is the distance among those two cities and we locate the shortest path way to complete the minimum switching motion. The difficulty can be describes as follows:

Given an undirected graph G = (V, E) where $V = \{V_1, V_2, ...V_n\}$ to find path $< V_1, V_2, ...V_n >$, such that for $i_j = \{1, ..n\} \forall j$, each summit from the graph can be visited once and only once.

**TEST SEQUENCE RESTRUCTURING**

Considering pharaonis algorithm have the optimistic feedback effect and convergence simply to a local optimum. Simultaneously, intersect machinist and mutation operator of inherent algorithm can develop diversity of solution. Henceforth genetic algorithm can be entrenched into the pharaonis algorithm [16][9]. Algorithm for Test Sequence reorganizing based on pharaonis algorithm and genetic algorithm is illustrated as follows:

Parameter initialization.:

Let $t = 0$, iteration times $E_t = 0$ and the maximal iteration times be $E_{t\max}, \eta_{ij}(t) = \frac{1}{d_{ij}}$

where $d_{ij}$ is the basting detachment between Test Sequences $i$ and $_j$.

Set the n pharaonis on the n basics.

Let the initialization in sequence for each edge on the directed graph be $\tau_{ij}(t)$,

where const denotes invariable and the initial time be $\tau_{ij}(0) = 0$ To encode

1. Let iteration times be $E_t \leftarrow E_t + 1$
2. Let the catalog number for ant taboo list be $k = 1$
3. Let the number of pharaonis be $k \leftarrow k + 1$
4. The character ant chooses the city $j(j \in \{C - tabu_k\})$ to move to according $P_{ij}^k(t)$
5. Modify the indicator of taboo list which indicates the original city that the ant attempts to shift to after pick and then add this city to the prohibited list for the ant
6. If set C is not visited systematically, that is, $k < n$, then go to step 4, else execute step 9
7. On the pharaonis character crossover and variation
8. Update the in sequence according $\tau_{ij}(t+n)$, $\tau_{ij}(t)$, $\tau^k_{ij}(t)$
9. If the conditions for loop terminates are fulfilled, that is, if iteration times subjects to $N > E_{t\max}$, jump opening the loop and output the results, else clear the forbidden list and jump step 2

$\tau^k_{ij}$, $\tau_{ij}(t+n)$, $\tau_{ij}(t)$ $\tau^k_{ij}(t)$ and $P^k_{ij}(k)$ is calculating according to [6].

**EXPERIMENTAL RESULTS**

Experimental results pedestal on ISCAS'85 benchmark circuits are executed. In these experiments, only the dynamic power rakishness is considered since it is the foremost term in the total power expenditure of CMOS circuits.

Table 1:

Results on Test Sequence restructuring

| Circuit Model | Beginning level Transitions | Closing level Transitions | Progress observed in percentage |
|---|---|---|---|
| 27-channel interrupt controller | 2962 | 1831 | 38.01 |
| 8-bit ALU | 7637 | 5499 | 28.01 |

| | | | |
|---|---|---|---|
| 32-bit SEC circuit | 16534 | 12456 | 24.64 |
| 16-bit SEC/DED circuit | 41100 | 28426 | 30.82 |
| 12-bit ALU and controller | 46588 | 30621 | 36.41 |
| 9-bit ALU | 111522 | 88735 | 21.35 |
| 32-bit adder/comparator | 284659 | 206532 | 30.98 |

Realized experimental results are given in Table 1. The very first line denotes the sort of the third column, the 2nd and signal denotes the total number of changes before using proposed criteria and that after using proposed criteria. The next column is the percent of power dissipation reduction.

It truly can be found that in the very best situation the proposed approach lessens the power dissipation for circuit 27-channel interrupt controller by 38.13%, while in the worst case, power dissipation for circuit 12-bit ALU and controller by 21.33%. The regular power dissipation is condensed by 30.05%. For several circuit, circuit transition activities are reduced by the proposed method somewhat.

## CONCLUSIONS

Because the technology has scaled down from sub-micron to nanometer region, energy minimization problem has become quite significant both during design and trial of VLSI circuits. In this research, a new approach predicated on pharaonis algorithm and genetic algorithm Optimization for Test Sequence restructuring is proposed for reduces the total energy dissipation through Test Sequence restructuring. This loom is an effective procedure for saving check power during testing will not the fault coverage and as it needs no additional DFT logic. The switching action for your proposed criteria is lowered compared with that received by restructure before. Tests have been performed on ISCAS'85 standard circuits and the results demonstrate that for several circuits, this restructuring approach may obtain an important lessening in test application power utilization. This approach doesn't involve at any given stage re-ordering of the of check cells that might be used for future work.

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