

Design and Analysis of Modified Fast Compressors for MAC Unit

Anusree T U¹, Bonifus P L²

¹PG Student & Dept. of ECE & Rajagiri School of Engineering & Technology

²Assistant Professor & Dept. of ECE & Rajagiri School of Engineering & Technology
Cochin, Kerala, India

Abstract — Multiplication and addition are the basic arithmetic operations which are important in several microprocessors and digital signal processing (DSP) applications. As the demand for high speed multipliers is continuously increasing, the studies related to the field of multipliers and adders are endless and still significant. Compressors can be used with the aim of reducing the power dissipation of multipliers without compromising their speed performance in which only multiplexer and basic gates are used. In this work, different topologies of 4:2 and 5:2 compressors are compared in terms of power delay product and number of transistors. Compressor topologies are simulated in 90nm Technology using Cadence Virtuoso schematic editor at 700mV power supply. The improved design can be used in multipliers with minimum delay than conventional ones which can be used in MAC units applied for DSP applications.

Keywords — 4:2 compressor, 5:2 compressor, Pass transistor logic, MAC unit

I. INTRODUCTION

The new trends in performance of handheld mobile communication and portable devices needs speed, area and power efficiency. Even before mobile era, power consumption has been the fundamental problem. Different ideas from device level to the architectural level and above were already proposed. However, there is no universal way to avoid tradeoffs between power, delay and area. So the techniques chosen by a designer must satisfy the application and needs.

Multipliers are one of the critical and compulsory components dictating the overall circuit performance as long as constrained by power consumption and computation speed. In multiplication process, the reduction of partial products contributes most to the overall delay, power and area. Compressors are employed to reduce the latency of this step. Hence compressors are a critical component of the multiplier circuit that greatly influences the overall multiplier speed. For high speed applications, a huge

number of compressors are to be used in multiplications to perform the partial product addition. Thus the studies related to the field of multipliers and adders are endless and still significant. Therefore, it is of great interest to develop high speed and low power compressors with minimum number of transistors.

Conventionally, partial product reduction has been carried out through the use of carry save adders consisting of rows of 3:2 counters, otherwise known as full adders. To increase the speed of multiplication higher order reduction schemes have been adopted. As an alternative to 3:2 counters, several higher order compressors were proposed. The 4:2 compressors, due to their ability to form regular interconnected cells structure are more popularly used. Higher order compressors such as 5:2, 6:2, etc., have also been employed in high precision multipliers to achieve greater performance. Fast 5:2 compressors are widely used for large word-size multipliers and multiply accumulators. As these compressors are used repeatedly in larger systems, improved design with lowest transistor count will contribute a lot towards overall system performance [2]-[4].

In this paper, section II briefly reviews the compressor architecture and concepts. The architectural details of the compressor designs and modified designs are given in section III. Simulated waveforms and comparison results are explained in section IV. Finally, section V concludes the report.

II. PREVIOUS WORK

Due to the reduction of switching energy per device caused by the continually shrinking feature sizes and negligible static power dissipation compared to dynamic power dissipation, logic styles has been prevailing as the technology for implementing low power digital systems. Different techniques have been used for power reduction and for reducing the number of transistors. Compressors are used in multipliers so as to increase the speed and these architectures can also lead to significant savings in the power consumed by the entire multiplier [1].

A 3:2 compressor adds carries and sum separately, such that all of the columns can be added in parallel without relying on the result of the previous column and creating a two output adder with a time delay that is independent of input sizes. Then the sum and carry can be recombined in a normal addition to form the actual result. This may take time delay and is more complicated.

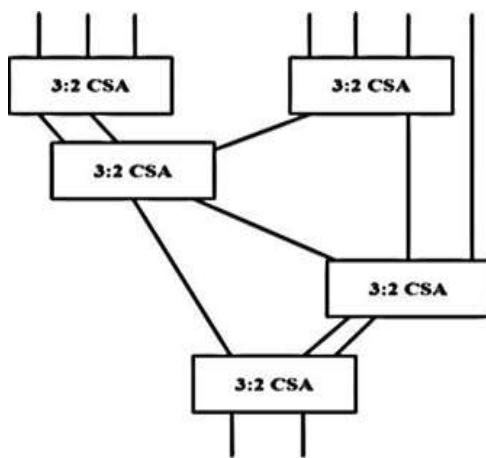


Fig. 1 Reduction tree

Compressors are used for accumulating the partial products in multiplication so as to speed up the operation. Full adders or 3:2 compressors were used for accumulation, in which 3 equally weighted bits were combined to produce two bits one carry with weight of $n + 1$ and the other sum with weight n . Each layer of the tree reduces the number of vectors by a factor of 3 to 2. Due to the ability to form regular interconnected cells structure 4:2 compressors are more popularly used. Higher order compressors such as 5:2, 6:2, etc., have also been employed in high precision multipliers to achieve greater performance. Fast 5:2 compressors are widely used for large word size multipliers and multiply accumulators [2]-[4].

A. 4:2 Compressors

The 4:2 compressor has 4 inputs X1, X2, X3 and X4 and 2 outputs Sum and Carry along with a Carry-in (Cin) and a Carry-out (Cout). The input Cin is the output from the previous lower significant compressor. The Cout is the output to the compressor in the next significant stage. The simplest implementation of 4:2 compressor is obtained by cascading two full adders in a hierarchical structure. Similar to the 3:2 compressor the 4:2 compressor is governed by the basic equation,

$$x_1 + x_2 + x_3 + x_4 + Cin = Sum + 2 * (Carry + Cout)$$

The standard implementation of the 4:2 compressor is done using two Full Adder cells as shown in Fig. 2, which is having a transistor count of 124 [2-4]. The disadvantages of this design are removed in enhanced designs. When the individual full adders are replaced into XOR blocks, the overall delay is dependent on the four XOR gates. The block diagram in Fig. 3 shows the design for the implementation of the 4:2 compressor using MUX and XOR gates. Conventional CMOS technology implementation of MUX and XOR gates are used in this design. It is having lesser number of transistors than conventional ones [4].

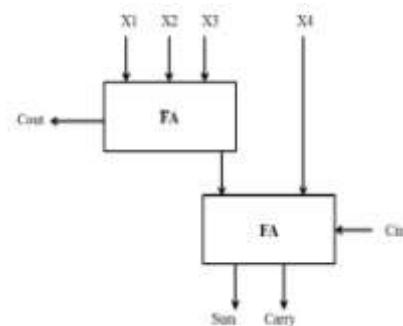


Fig. 2 Conventional 4:2 compressor

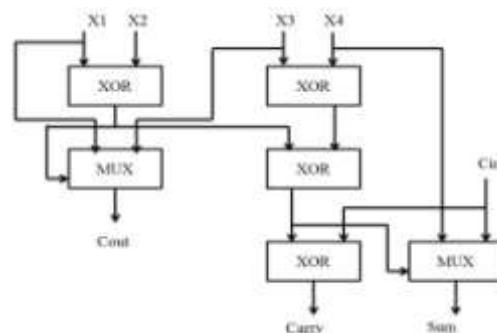


Fig. 3 4:2 compressor design II

B. 5:2 Compressors

The 5:2 Compressor block has five inputs X1, X2, X3, X4, X5 and 2 outputs, Sum and Carry along with two input carry bits (Cin1, Cin2) and 2 output carry bits (Cout1,Cout2). Five inputs are primary input and the rest are two input carries which receive their values from the previous stage of one bit lower in significance. All the seven inputs as well as output Sum bit have the same weight. The input carry bits are the outputs from the previous lesser significant compressor block and the output carry are passed on to the next higher significant compressor block. The other three output bits weight one bit higher order. Various structures for 5:2 compressors already proposed. Equation below is the basic equation that governs the function of the 5:2 compressor blocks.

$$x_1 + x_2 + x_3 + x_4 + x_5 + \text{Cin}_1 + \text{Cin}_2 = \\ \text{Sum} + 2 * (\text{Carry} + \text{Cout}_1 + \text{Cout}_2)$$

The conventional implementation of 5:2 compressor is shown in Fig. 4. Hierarchical structure of cascaded full adder cells is used in this conventional circuit. The speed and the number of transistor count are not favourable for a fast and area efficient design. In the design of 5:2 compressors Cout1 must be independent of Cin1 as well as Cin2. In addition, Cout2 must be independent of Cin2. The delay increases as the signal propagates from one compressor to the other. It is the main concept of performance development of compressors. Thus the dependency of Cout2 to Cin1 causes carry to propagate to the third compressor. The method in Fig. 3 is to make the Cout2 independent of Cin1. This will limit the carry propagation to one compressor. Here the XOR* gate is replaced by pass transistor logic. CGEN blocks have been used to generate Cout1 and Cout2 signals using CMOS technology [4].

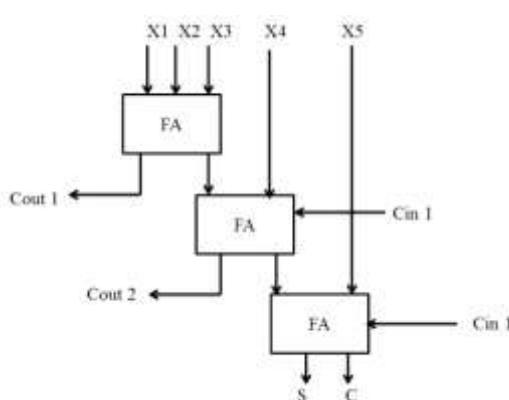


Fig. 4 Conventional 5:2 compressor

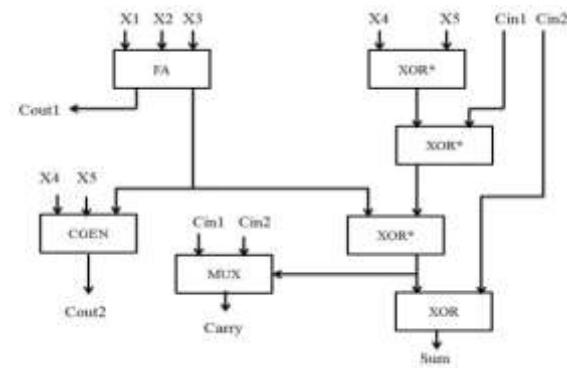


Fig. 5 5:2 compressor design II

III.MODIFIED COMPRESSORS

The block diagram in Fig. 6 shows the design for the implementation of the 4:2 compressor using MUX and XOR. Here the XOR using pass transistor logic is implemented as shown in Fig. 7. It is a six transistor implementation, were the transistor count is reduced.

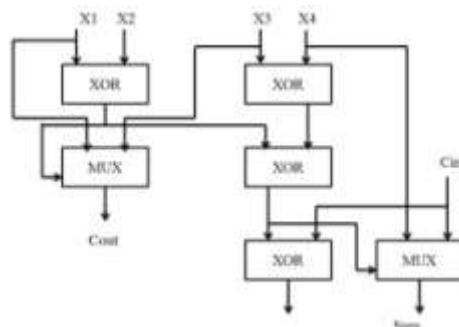


Fig. 6 4:2 compressor design III

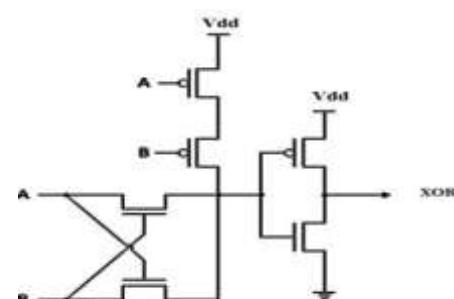


Fig. 7 XOR gate with pass transistor logic

The block diagram in Fig. 8 shows the design for the implementation of the 4:2 compressor using MUX and XOR-XNOR. However, like in the case of 3:2 compressor, the fact that both the output and its complement are available at every stage, is neglected. Here the XOR is replaced with MUX* which provides improvement in speed of the design. Also the MUX block at the Sum output gets the select bit before the inputs arrive and thus the transistors are already switched by the time they arrive.

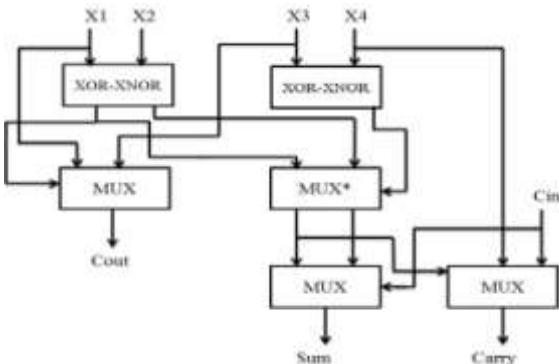


Fig. 8 4:2 compressor design IV

The 5:2 compressor architecture shown in Fig. 9 is an improved architecture of existing ones. Changes to internal equations of the 5:2 compressor are made to eliminate final NOT gates of the CMOS FA. The power dissipation as well as the operational speed can be improved. To achieve this goal, XNOR gates are used instead of XORs of the second stage of the architecture. This design uses 82 transistors in its architecture. In this architecture, FA-NOT is CMOS full adder with its final NOT gates have been eliminated. Carry generator modules which is also used in design II have been used here to produce Cout1 and Cout2 output signals. In addition, outputs of the XOR gates have been fed to inputs of the XNOR gates. In this way, outputs of the XNOR gates are negation of what it was before for conventional 5:2 compressors and by replacing a FA-Not instead of a FA there is a valid Sum and Carry signals and the XNOR module is shown in Fig. 10.

The design IV is a modified architecture shown in Fig. 11, changes have been made to efficiently use the outputs generated at every stage, by replacing few XOR blocks with MUX blocks. The select bits to the multiplexers in the critical path are made available much ahead than input so as to reduce the critical delay.

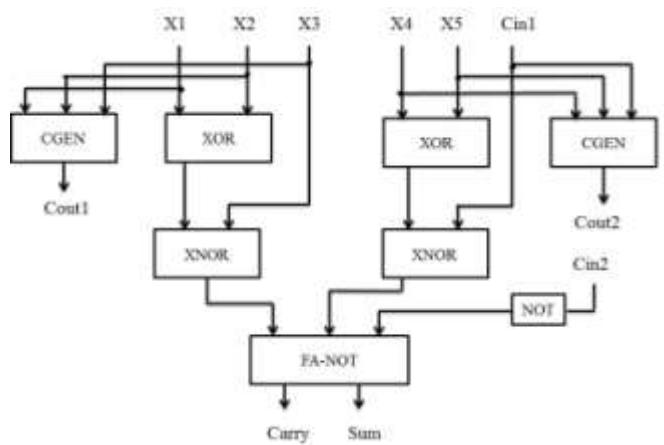


Fig. 9 5:2 compressor design III

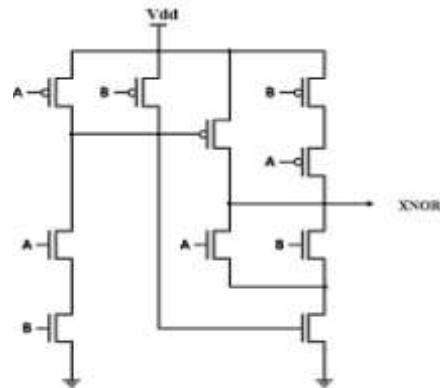


Fig. 10 CMOS implementation of XNOR gate

If the output of the multiplexer is used as select bit for another multiplexer, then it can be used efficiently in similar manner because the negation of select bit is also required in the design and an extra stage to compute the negation can be saved. Similarly replacing the XOR block in the second stage with a MUX block as shown in Fig. 12 reduces the delay because the select bit X3 is already available and the time taken for the transistor switching to take place is done in parallel with the computation of the inputs of the block. In all the general implementations of the XOR or MUX block, the output and its complement are generated. Existing architectures is not using this advantage. In this design the outputs are utilized efficiently by using multiplexers at select stages in the circuit. Also additional inverter stages are eliminated. This in turn contributes to the reduction of delay, power consumption and the transistor count is considerably less.

IV. RESULTS AND DISCUSSIONS

Four different architectures of 4:2 and 5:2 compressors are simulated in cadence virtuoso schematic editor at 700mV supply voltage. Design I of each compressor type is conventional designs. Design III and IV of 4:2 and 5:2 compressors are modified designs. The average power, worst case delay and transistor count were calculated. The output waveforms of optimized designs are seen in Fig. 11 and Fig. 12. The results and inferences obtained from the simulation results were explained in this section with the help of tabular and graphical comparisons.

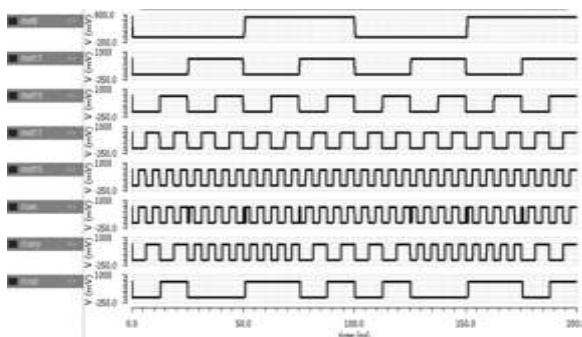


Fig. 11 Waveform of 4:2 compressor design III

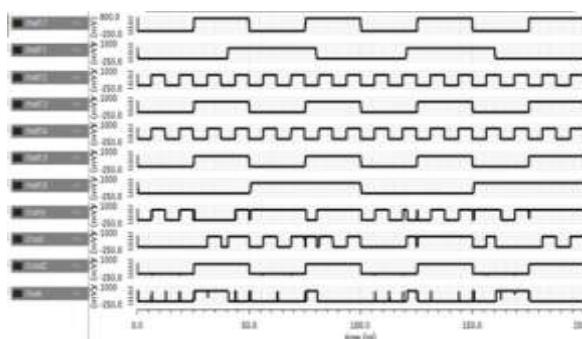


Fig. 12 Waveform of 5:2 compressor design IV

The comparison of power in terms of micro watts , delay in Nano second and their PDP, that is the power delay product and number of transistors of each designs of both 4:2 compressors and 5:2 compressors are shown in Table I and Table II. And the corresponding graphs are shown in Fig. 13 and Fig. 14 respectively.

TABLE I
COMPARISON TABLE OF 4:2 COMPRESSOR

Types of compressor	Power (μW)	Delay (nS)	PDP (fJS)	Transistor count
Design I	16.98	336	5.705	124
Design II	22.17	110	2.482	128
Design III	5.672	62.1	0.353	72
Design IV	8.89	155.6	1.383	96

TABLE III
COMPARISON TABLE OF 5:2 COMPRESSOR

Types of compressor	Power (μW)	Delay (nS)	PDP (fJS)	Transistor count
Design I	16.98	336	5.705	124
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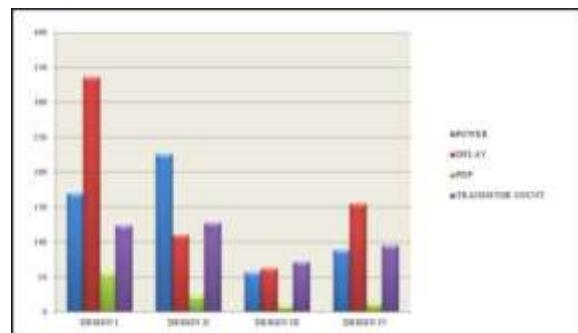


Fig. 13 Comparison table of 4:2 compressors

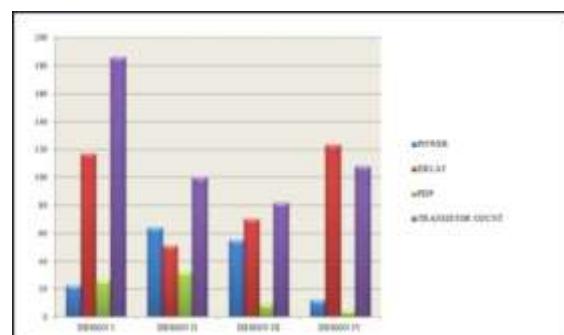


Fig. 14 Comparison table of 5:2 compressors

From the observed results of 4:2 and 5:2 compressors which is obtained from Cadence simulation is plotted in Fig. 13 and Fig. 14 respectively (PDP is scaled by multiplying with 10

in the plot for proper view). Table I and Table II shows that there exists a trade-off between power, delay and number of transistors. From the observed designs third design of 4:2 compressor have the minimum PDP, which is the power delay product. The transistor count is also less compared to other designs. The use of pass transistor logic reduced the transistor count in this design III. From the observed designs of 5:2 compressors the design IV has the minimum PDP. The transistor count is also less compared to other designs, thus the area can be optimized.

V. CONCLUSIONS

In this work, PDP and transistor count of four different designs of 4:2 compressors and 5:2 compressors are compared in Cadence with 90nm Technology at 700mV. The Cadence simulation results shows that the third design of 4:2 compressors and the fourth design of 5:2 compressors are most efficient, which are modified versions of existing designs. It is concluded that among the four 4:2 compressor simulated design, the third design is most energy efficient one and there exists a tradeoff between PDP and transistor count but the hardware cost is reducing. Among the four 5:2 compressor simulated design, the third design has minimum transistor count and consequently is the most energy efficient one with minimum PDP. That is, by lowering the supply voltage and optimizing the design, efficiency can be improved without much area overhead. As a future work these compressors can be used in multipliers which can be used in MAC units for high speed applications like DSP, WSN etc.

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