Designing Nanotechnology Based QCA Full Adders

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Abstract *Nanotechnology based QCA basic logic layouts work well while simulating on QCA Designer software. The design of half adders has been reported by various researchers and most of the circuit combinations produce excellent results on simulation. Although design of QCA full adders has been reported by a large number of researchers but the simulation results on most of the circuits fail to produce claimed outputs as such the carry forward work is becoming difficult. There are certain difficulties in producing desired simulation results while joining two half adders to design full adder. The main cause for the problem seems to be the mismatch of input data, when earlier stage data is combined with the forward stage. We have tried to study some full adder designs on the basis of simulation results to move forward with our own designs for the purpose. With analysis of few reported adders we have proposed two full adder circuit layout designs with analysis for efficient implementation and future improvements.*

Keywords: *QCA; Tunneling; Microelectronics; Boolean Algebra; Electrostatic Noise; QCA Designer; Full Adder; Simulation Result; Single Layer Layout.*

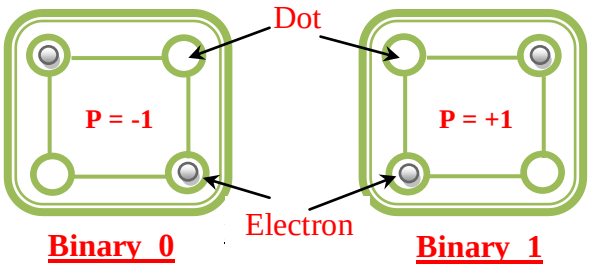
1. INTRODUCTION

The system of device design based on electron positioning gave birth to concept of quantum-dot in early eighties. A quantum-dot thus can be defined as a nano-scale vessel in which an electron can be trapped. Dot as such can be termed as a potential well or ring in which a sufficiently low energy electron can be trapped. There are several ways of implementing quantum-dot and the tested and commonly used is Aluminum metal-dot developed with the help of electron lithography. The electrons in cell-dots can crossover through a technique known as Dolan bridge technique [1] that physically embeds a capacitor junction between the dots in a quantum cell. As the repulsive force is encountered by an electron from the adjacent electron it tunnels through Dolan bridge junction to the adjacent vacant dot.

The dots produced with the help of electron beam lithography are not having a similar shape but varied shapes depending on the process and application. There are various processes of producing these devices and one of big challenges to achieve the objective is the precise location of quantum dots at the desired locations. Self organization is one of these processes and occurs when molecules of one crystal structure is deposited on the top of another. The lattice structure difference results in high stresses at the point of contact as such the material tends to clamp up at the point of contact in a manner of depositing oil on water. Although this process can produce dots of incredibly small size but one big problem is that the dots are not located at desired places.

1.1 Quantum-dot Cell

A cell is a device used to store and transmit data using electrons and the Columbic interactions. The electrons change orientations from 0 (zero) to 1 (one) or vice-versa by changing positions through electron tunneling. A four dot quantum cell with two excess electrons is shown in Figure (1) representing two binary states of 0 (zero) and 1 (one) and the arrangement will always place the electrons in the opposite corner or antipodal positions due to their repulsive force on each other. C. S. Lent, Almani and W. Porod at Notre Dame University [2, 3, 4, 5] proposed a wireless two state quantum device cell of five dots as shown in Figure (2). The modal similar to four dot cell modal yields two states of equal energy in the cell.



1.2 Cell Working

The electrons in the cell always have the antipodal sites in both states of logic one (1) and logic zero (0) but the alignments are opposite as shown in figure (2) and figure (3).

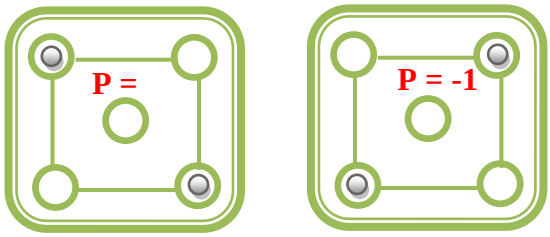


Figure (2)

If two cells are brought close to each other they get aligned in the same direction due to inter columbic interaction as shown in Figure (4). The cells assume the order of lower energy in the system. In other words if a cell among two adjacent cells is brought to a state of '1' or

'0' the adjacent cells will also get into same state. The carriage of state from one cell to its adjacent cell is said to have transmitted data and if a number of cells are placed adjacent to each other the data will travel from one end to other. Although no current flows but the conduction has taken place. This sort of conduction is the basic principle behind the working of quantum-dot cell devices. The shift of electron from one dot to other is electron from one dot to other is facilitated with the help of tunnel capacitor junction between the dots. This technique known as Dolan bridge technique physically embeds a capacitor junction between the dots in a quantum cell. As the repulsive force is encountered by an electron from the adjacent electron it tunnels through Dolan bridge junction to the adjacent vacant dot. The Dolan bridge junction between the dots in a quantum cell is demonstrated in Figure (4).

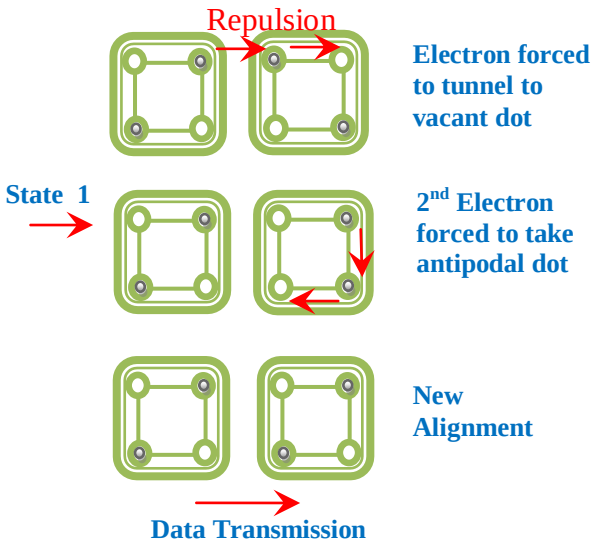


Figure (3)

2. ASSEMBLING QCA DEVICES

On the basis of the basic properties of the quantum cells developed at Notre Dame University different algorithms have been designed to explore the possibilities of the devices with the help of software simulations. We have also studied and analyzed different logical device layouts with the help of QCA Designer software tool to arrive at some definite robust conclusions. As discussed above the quantum-dot cells arranged in a line produce a sort of conduction, this assembly of cells is termed as wire. A wire simulation is carried out by arranging a number of cells in a line and making the one end as input with respect to the other. Second important thing is to draw several output lines from a single input, this is termed as Fan-out. A fan-out is extension of the wire layout design and the only difference is to watch the similar waveform appearing at different output lines. The logic NOT operation in QCA is performed in different ways and two ways to achieve this objective have been demonstrated in Figure (5).

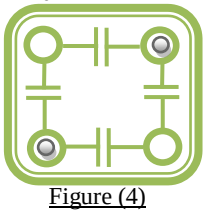
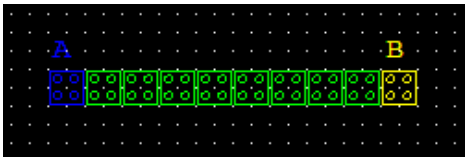
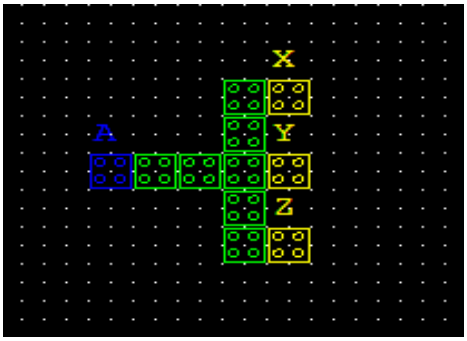


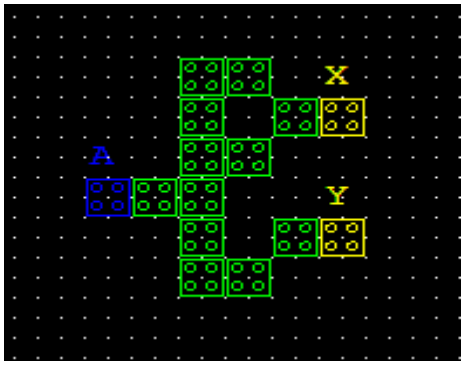
Figure (4)



A Wire



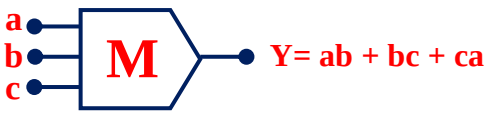
Fan out



NOT options

Figure (5)

Fundamental gate for the QCA exploration has been identified as the majority gate. It has three inputs and an output and its output is high when at least two of its inputs are high. The symbol and logic expression of the gate is given below:

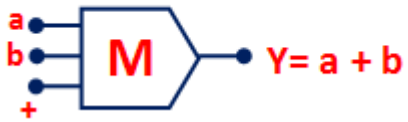


Majority Gate Symbol

This gate is implemented by few quantum cells and has been demonstrated in the Notre Dame laboratory. The gate has a versatile property of acting as AND and OR gate with simply fixing one of its inputs. Let us assume the c input of the above to be at logic one i.e. c = +1 the Boolean expression for the above gate becomes

$$Y = ab + a + b$$

$$Or\ Y = a(b+1) + b \quad since\ b+1 = 1$$
$$Therefore\quad Y = a + b \qquad (OR\ gate)$$



In the similar way if the c input of the majority gate is fixed to logic '0' zero i. e. c = -1 the Boolean expression for the gate becomes

$Y = ab + 0 + 0$

$Or \quad Y = ab \quad (AND\ gate)$

Hence having NOT and the Majority gate to design OR and AND gates one has ample liberty to implement any kind of Boolean expression used for circuit design in digital electronics. Cell layout and simulation result for AND, OR and Majority gates has been reported by maximum researchers on five cell assembly. We have observed some noise distortion in the output as such an addition of one more cell at output stage was observed to produce robust results. The layout of the majority gate is presented in figure (6) below:

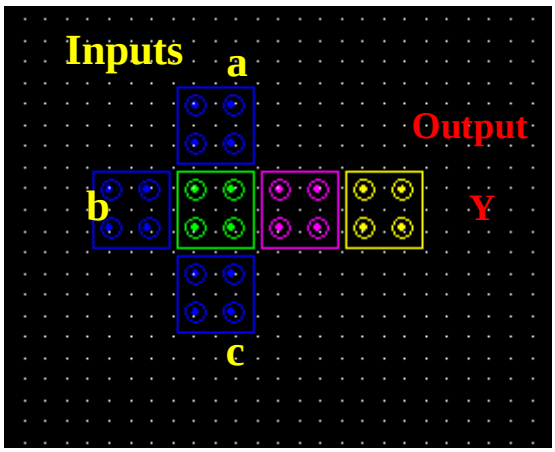


Figure (6)

Implementation of other logic gates like NAND and NOR can be simply designed by putting a NOT gate at the output of AND and OR gates respectively. The symbolic representation along with Boolean expression for these gates is given in Table (1). The main problem in the design arises when we start simulations for the Excusive-OR and Exclusive-NOR gates. These gates as we know are designed with the assembly of few gates, the layout imbalance and the clocking zone extensions produce interference in the output wave forms.

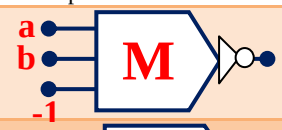
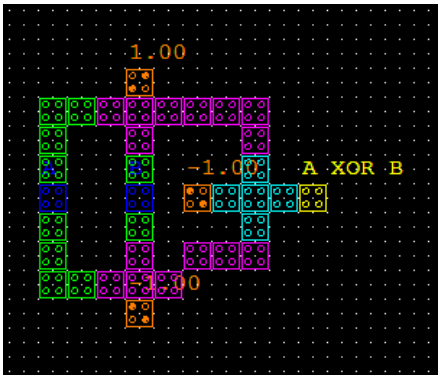
NAND Gate	
NOR Gate	

Table (1)

The Excusive-OR gate has been proposed with various layouts by different researchers and prior to this study we have reported some analyzed layouts [6], two among them will be demonstrated to carry forward the work for the design of full adders. The layouts along with their simulation results on QCA Designer are presented in figure (7-a) and (7-b).



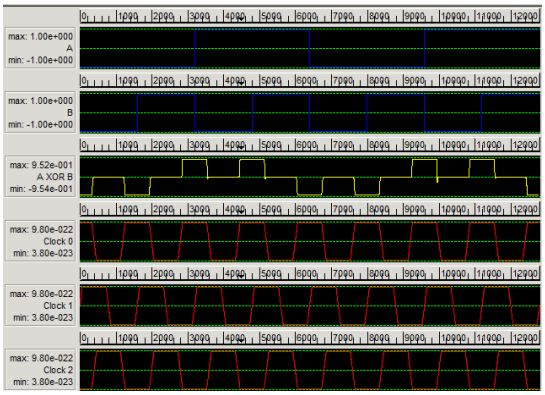
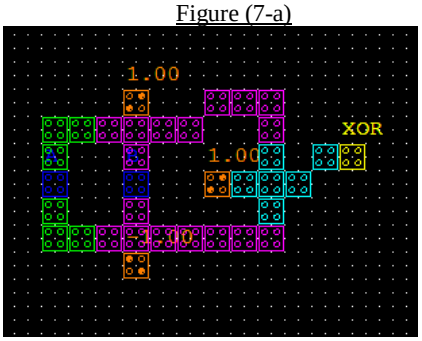


Figure (7-a)



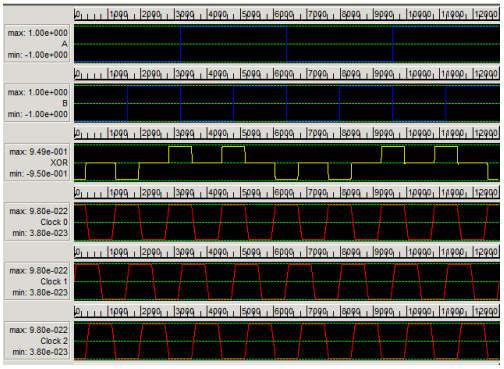


Figure (7-b)

In digital electronics we usually design full adders by connecting two half adders to generate the output signal. While designing QCA full adders using same techniques number of problems arise in combining the signals of different stages due to mismatched clock. In the present study we have tried different techniques to overcome this problem for the layout designs of full adder.

3. STUDY OF ADDER LAYOUTS

3.1 Designing Half Adders

The traditional way of designing adders is based on assembling half adders. In digital electronics the Boolean expression is derived for the required outputs and the circuit implementation is followed after minimization of the Boolean expressions. The binary sum of two bits can be simply got by an Exclusive-OR gate and the carry will be handled by a separate AND gate. The circuit assembly is known as Half Adder and its implementation using QCA is also simple because of the involvement of single stage of two gates. Here we move forward with the Exclusive-OR gates discussed in the previous section to convert them to half adders. Let us take the Exclusive-OR gate based on Boolean expression represented by equation (1) given below:

$$Sum = (\overline{AB}).(A + B) \quad \dots (1)$$

$$Carry = AB \quad \dots (2)$$

Where A and B are the two input bits. The expression for the required carry can be simply generated by same assembly with a minor cell increase as the NOT form of AB is already present in the equation (1). The design layout of this Half Adder is given in Figure (8-a) and its simulation result is presented in Figure (8-b). The results indicate perfect working of the layout with a minimum latency and a low count of cells for this implementation. Other way of designing the Half Adder is based on the Boolean expression represented by equation (3) given below:

$$Sum = \overline{(\overline{A + B}) + (AB)} \quad \dots (3)$$

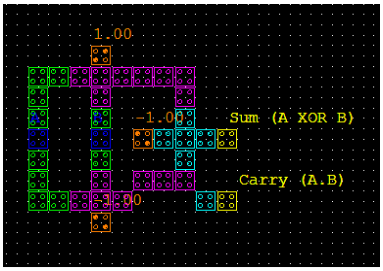


Figure (8-a)

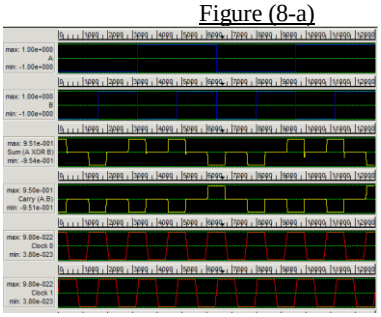


Figure (8-b)

The generation of carry is again simple as the AB component is present in the assembly of the layout for this Exclusive-OR gate. The circuit layout is presented in Figure (9-a) along with its simulation results on QCA Designer in Figure (9-b). The results in this case are almost same but this layout gives indication of more stability against electrostatic noise and has further advantage of occupying a bit lesser area in comparison to the above layout. These two layouts can form the basis for the design of Full Adders based on the traditional way of assembling two Half adders for the purpose. There are alternative ways too for designing Full Adders without using the traditional method. The methods arise due to Boolean alternative expression generation.

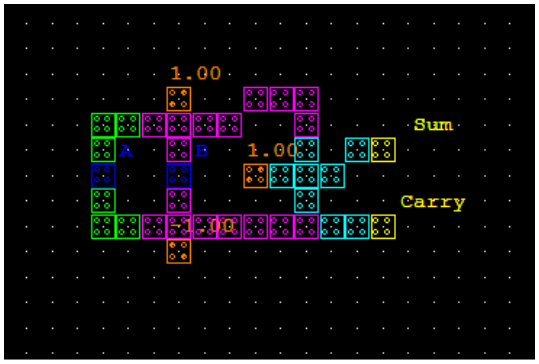


Figure (9-a)

The circuit algebra is used to convert the Boolean expressions of Full Adder to desired form for implementation. In QCA implementation a number of researchers have tried to look for the alternative of Full Adder layouts and before moving forward with our designs based on traditional method we will like to have survey of the proposed alternatives.

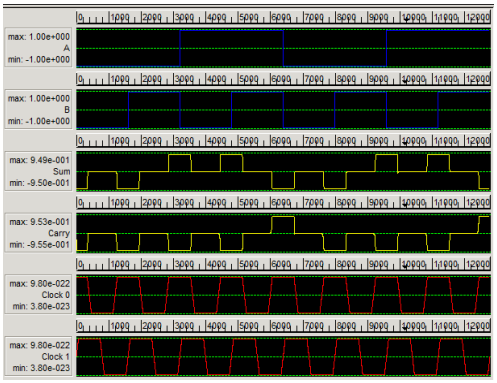
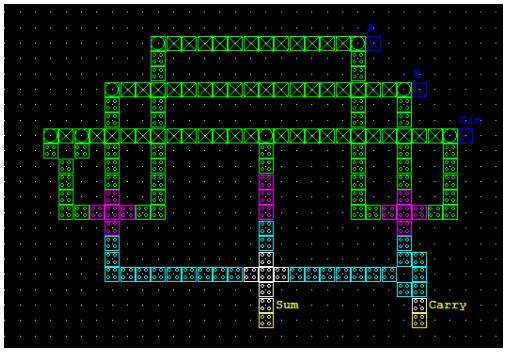


Figure (9-b)

3.2 Zhang Full Adder Layout

A number of Full Adder layout designs have been reported using different techniques by various researchers. One of such circuit layouts is proposed by Zhang et. el. [7] and is presented in Figure(10). The layout has been designed on the basis of reduced majority gates approach and appears to be a balanced compact assembly. We have analyzed the layout with the same algorithm and software (QCA Designer) and found the results inconsistent with the projected hypothesis. This multilayer layout was found to have lot of sneak noise paths as such an alternative single layer layout based on same logic was again simulated for crosscheck observations. The layout along with its simulation results is shown in figure (11-a) and figure (11-b) respectively.



Figure(10)

The analysis of the output yields correct behavior for carry signal but failure in producing desired signal for the sum of this adder circuit on QCA Designer software. The implementation algorithm for this adder is based on the following Boolean expressions:

$$Sum = MV(\overline{MV(A, B, Cin)}, Cin, MV(A, B, \overline{Cin})) \quad \dots (4)$$

$$Carry = MV(A, B, Cin) \quad \dots (5)$$

These equations present a correct Boolean method of designing reduced majority gate based full adder, but the desired outputs are not produced even after changing orientation of layout from two layer to single layer.

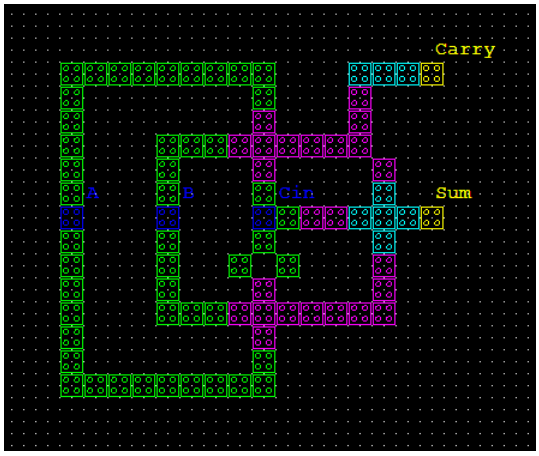


Figure (11-a)

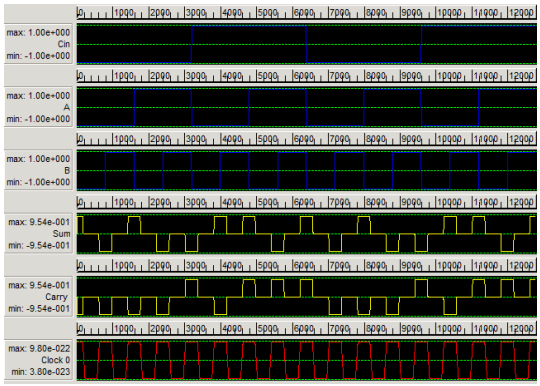


Figure (11-b)

The result clearly suggest the revisit of the projected hypothesis to ascertain the reliability of the simulation software regarding its fitness for production of desired results under reduced majority logic conditions.

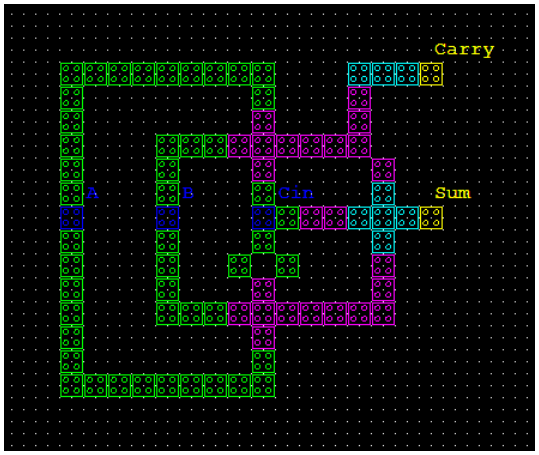


Figure (11-a)

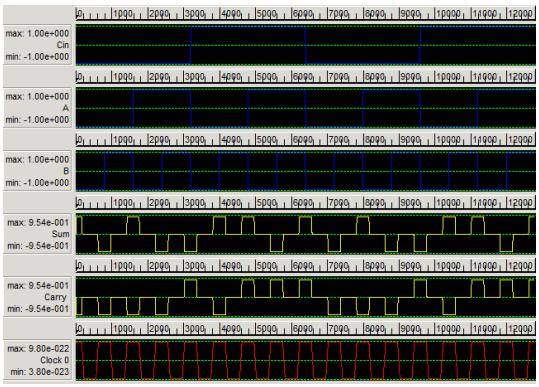


Figure (11-b)

The result clearly suggest the revisit of the projected hypothesis to ascertain the reliability of the simulation software regarding its fitness for production of desired results under reduced majority logic conditions.

3.3 Cho Full Adder Layout

Another layout designed on the basis of reduced majority logic has been reported by [8] and is shown in figure (12). The design assembly was simulated on QCA designer software and produced results as shown in figure (12-a). Although we have not changed the orientation of the layout from multilayer to single layer but surely the hope of improvements in the results with QCA Designer software is very low.

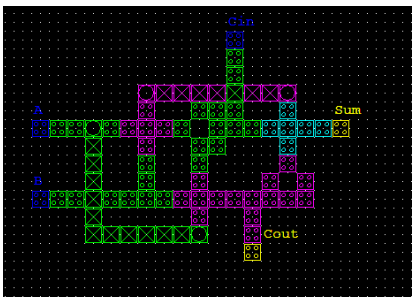


Figure (12)

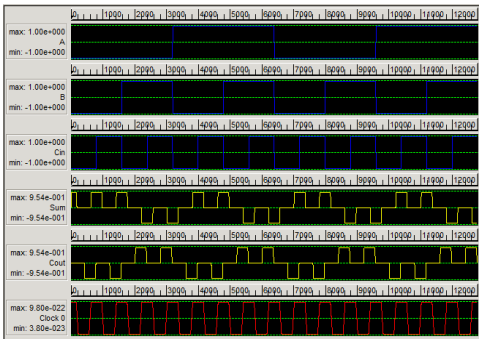


Figure (12-a)

3.4 Simulation of Few More Layouts

Few more configurations based on reduced majority logic by Walus et. el. [9] were also tested by us with the help of same software and found producing inconsistent results on simulation. Although the designs seem to be based on reduced majority gate equations but the result deviations suggest need of more study on both the robustness of software and the projected hypothesis. The layout assembles include designs proposed in [10, 11, 12].

4. PROPOSED FULL ADDER LAYOUTS

Based on our previous work in [6] on the design half adders we have analyzed and simulated two layout configurations for the implementation of full adders and we will explain their analysis one by one in the following sub-sections.

4.1 Proposed Layout -First

This layout is based on the half adder design of figure (7-b). There is certainly a bit of complexity in generating the carry signal because it composes of two signal bits of different stages. The layout is given in figure (13-a) and its simulation results are given in figure (13-b). This layout is designed with the help of Boolean equations of traditional full adder circuits in microelectronics. Although the layout has a correct base of the Boolean algebra but the simulation results produce noisy result for the carry signal. Red circles in figure (13-b) have been drawn to show the signal variations at different places in the simulation output.

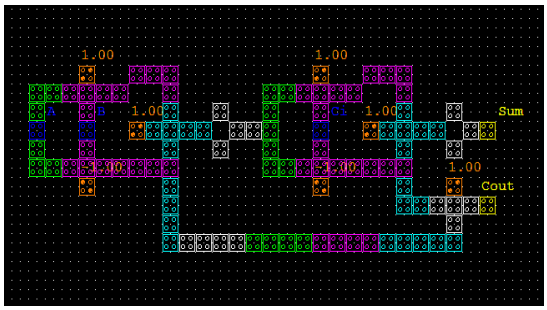


Figure (13-a)

The signal waveform for the sum signal is correct representation of the full adder layout with some propagation delay but the carry signal although incorrect in only one combination cannot be regarded as a valid result. This suggests a valid reason for looking into the robustness of the QCA Designer software for simulating the layout designs. We have tried a number of variations in this layout but could not generate the desired results on simulation for this case.

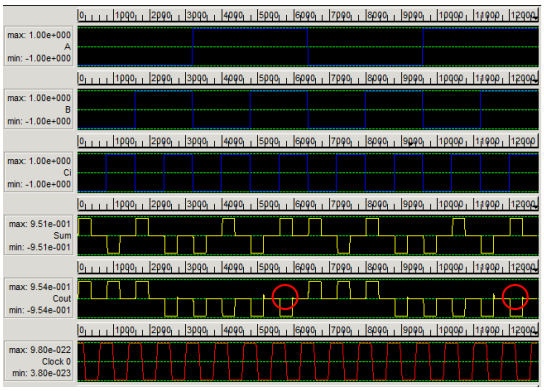


Figure (13-b)

4.2 Proposed Layout -Second

Projection from the above sections about the validity of QCA Designer software is only an option as the simulated results do not appear to be inconsistent. In maximum simulations the software produces convincing outputs. However some apprehensions regarding few outcomes needs to be thoroughly investigated. An alternative layout based on same Boolean logic but using half adder of figure (8-a) was designed and simulated by us for desired output waveforms. This layout is given in figure (14-a) and its simulation results on QCA Designer are shown in figure (14-b).

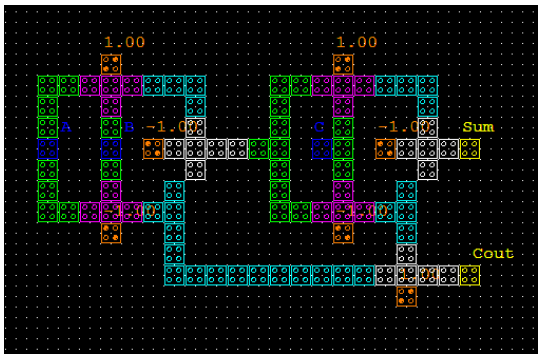


Figure (14-a)

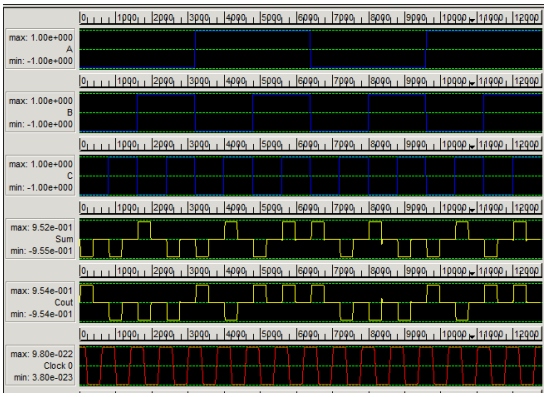


Figure (14-b)

The simulation results are completely consistent with the theory concept of full adders in Boolean algebra. Although circuit proposed layouts and some analyzed layouts of the

previous section are perfectly according to Boolean or reduced majority logic but the results vary on simulation with QCA Designer software. Hence the evidence of sneak noisy paths proposed in [14, 15] in the design of QCA layouts need to be investigated.

5. DISCUSSION & CONCLUSION

In this study we have not only proposed our version of QCA based full adder layout designs but also analyzed a good number of previously projected layouts to move ahead with concrete information regarding their working status on simulation. Our study suggests that the circuit layout comparison on the parameters of layout area, reduced majority logic, /Boolean logic, propagation delay, cell count or temperature are of secondary importance against considerations of working conformity with the help of some elegantly designed software. Although all the basic circuit layouts perform well on QCA Designer but to ascertain causes of varied results on simulation of full adders needs a through revisit in terms of both, the projected layouts as well as simulation software. We have already started our work regarding alternative options of layout designs with lesser noise crossover and simulation stability. The observations are projected for the fellow researchers to strive for the solution of the uncertainties regarding this promising field of technological development in future.

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