Low Power Dissipation for High Fault Coverage using BIST
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Abstract— A low hardware overhead scan based BIST test pattern generator (TPG) that reduces switching activities in circuit under test (CUTs) and also achieve very high fault coverage with reasonable length of test sequence is proposed. When the proposed TPG used to generate test patterns for test-per-scan BIST, it decreases the number transitions that occur during scan shifting and hence reduces the switching activity in the CUT. The proposed TPG does not require modifying the function logic and does not degrade system performance. The proposed BIST comprised of three TPGs: Low transition random TPG (LT-RTPG), 3-weight weighted random BIST and Test patterns generated by the LT-RTPG detect the easy-to-detect faults and remain the undetected faults can be detected by the WRBIST. The 3-weight WRBIST is used to reduce the test sequence lengths by improving detection probabilities of random pattern resistant faults (RPRF).

Index Terms— Built-in self-test (BIST), switching activity, low power testing, test pattern generator.

I. INTRODUCTION

Modern design and package technologies make external testing increasingly difficult and the built-in self-test (BIST) has emerged as a promising solution to the VLSI testing problem. BIST is a design for testability methodology aimed at detecting faulty components in a system by incorporating test logic on-chip. The main components of a BIST scheme are the test pattern generator (TPG), the response compactor, and the signature analyzer. Among various BIST schemes, pseudo random BIST is most widely used since it is most economical. Unlike deterministic stored pattern BIST, which requires the high hardware overhead due to the memory devices required to store precomputed test patterns, pseudo random BIST , where test patterns are generated by pseudorandom pattern generators such linear feedback shift registers (LFSRs) and cellular automata (CA), requires very little hardware overhead. However, BIST using only pseudo random patterns doesn’t provide high fault coverage due to the existence of random-pattern-resistant faults (RPRF). The random pattern test length required to achieve high fault coverage is often determined by only few hard-to-detect faults. These faults also called RPRFs because they escape most random test patterns.

Several techniques have been suggested for enhancing the fault coverage achieved with BIST. These techniques can be classified as; (1) Modifying the circuit under test by test point insertion or by redesigning the CUT to improve the fault detection probabilities. The drawback of these techniques is that they generally add extra levels of logic to the circuit that can degrade system performance. Moreover, in some cases, it is not possible or not desirable to modify the function logic (e.g., macro cells, cores, legacy designs). 2) Mixed-mode testing where the circuit is tested in two phases. In the first phase, pseudo-random patterns are applied. In the second phase, deterministic patterns are applied to target the undetected faults. Storing deterministic patterns in a read-only memory (ROM) requires a large amount of hardware overhead. (3) Weighted pseudo-random patterns, where the random patterns are biased using extra logic to increase the probability of detecting RPRFs. In weighted random pattern testing, the outputs of test pattern generator (TPG) are biased to generate test sequences that have nonuniform signal probabilities to increase detection probabilities of RPRFs that escape pseudorandom test sequences, which have a uniform signal probability of 0.5. Random pattern use Markov sources to exploit spatial correlation between state inputs that are consecutively located in the scan chain. A 3-weight weighted random BIST (3-weight WRBIST) can be classified as an extreme case of conventional weighted random pattern testing BIST. However, in contrast to conventional weighted random pattern testing BIST where various weights, e.g., 0, 0.25, 0.5, 0.75, 1.0, can be assigned to outputs of TPGs, in 3-weight WRBIST, only three weights, 0, 0.5, and 1, are assigned. Since only three weights are used, circuitry to generate weights is simple; weight 1 (0) is obtained by fixing a signal to a 1 (0) and weight 0.5 by driving a signal by an output of a pseudorandom pattern generator, such as an LFSR. Weight sets are calculated from test cubes for RPRFs.
 Though the attainment of high fault coverage with practical lengths of test sequences is still one major concern of BIST techniques, reducing switching activity has become another important objective. It has been observed that switching activity during test application is often significantly higher than that during normal operation. The correlation between consecutive random patterns generated by an LFSR is low; this is a well-known property of LFSR generated patterns. On the other hand, significant correlation exists between consecutive patterns during the normal operation of a circuit. Hence, switching activity in a circuit can be significantly higher during BIST than that during its normal operation. Since heat dissipation in a CMOS circuit is proportional to switching activity, a CUT can be permanently damaged due to excessive heat dissipation if switching activity in the circuit during test application is much higher than that during its normal operation. Heat dissipated during test application is already influencing the design of test methodologies for practical circuits.

Metal migration (electro migration) causes erosion of conductors and subsequent failure of circuits. Since temperature and current density are major factors that determine electro migration rate, elevated temperature, and current density caused by excessive switching activity during test application will severely decrease reliability of CUTs. This is even more severe in circuits equipped with BIST since such circuits are tested frequently.

To test a bare die, power must be supplied during the period of test through probes, which typically have higher inductances than power and ground pins of the circuit package. Hence, the bare die under test will experience higher power/ground noise which is given by $\frac{L}{d}\frac{dI}{dt}$, where $L$ is the inductance of power and ground line and $\frac{dI}{dt}$ is the rate of change of current flowing in power and ground lines. Excessive power/ground noise can erroneously change the logic state of circuit lines causing some good dies to fail the test, leading to unnecessary loss of yield. The rest of this paper is organized as follows. The techniques that are used in this paper to reduce switching activity during BIST are illustrated in Section II and III. Section IV briefly introduces the serial fixing 3-weight WRBIST. The architecture of the proposed TPG and the outline of algorithm used to design the proposed BIST TPG are described in Section V. A technique to minimize hardware overhead for implementing the proposed BIST TPG for circuits with multiple scan chains is presented in Section VI. Finally, Section VII presents the conclusions.

I. LOW TRANSITION RTPG

A. Overview of LT-RTPG design

The LT-RTPG reduces switching activity during BIST by reducing transitions at scan flip-flops during scan shift operations. Fig. 1 shows an architecture called LT-RTPG. The LT-RTPG is comprised of an r-stage LFSR, a k-input AND gate, and a toggle flip-flop (T flip-flop). Hence, it can be implemented with very little hardware. Each of $K$ inputs of the AND gate is connected to either a normal or an inverting output of the LFSR stages. If large $K$ is used, large sets of neighboring state inputs will be assigned identical values in most test patterns, resulting in the decrease fault coverage or the increase in test sequence length. Hence, LT-RTPGs with only or 3 are used. Since a flip-flop holds previous values until the input of the T flip-flop is assigned a 1, the same value $v$, where $v \in \{0,1\}$, is repeatedly scanned into the scan chain until the value at the output of the AND gate becomes 1. Hence, adjacent scan flip-flops are assigned identical values in most test patterns and scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations (a capture cycle occurs at every cycle), the LT-RTPG can reduce heat dissipation during overall scan testing. Various properties of the LT-RTPG are studied and a detailed methodology for its design is presented in [23].
B. Analysis of LT-RTPG

The combinational part of a sequential circuit can be viewed a collection of (overlapping) output cones, where an output cone \( \Omega_j \) is composed of all the logic and inputs (primary and state) that form the fan-in of \( j \)th output. A pair of inputs are said to be compatible if there exists no circuit cone to which they both belong. For faults such as stuck-at, any correlation between the values applied to a pair of compatible inputs does not reduce the fault coverage for any given test length.

Consider a full scan circuit with a single scan chain. Let the span \( S_j \) of cone \( \Omega_j \) be the distance between the first and last flip-flops in the scan chain as shown in Fig (cone fig), whose outputs drive the state inputs of the cone. If the \( \alpha \)-th and \( \beta \)-th flip-flops of the scan chain drive the first and last flip-flops of the \( \Omega_j \), then \( S_j = \beta - \alpha + 1 \). Then span \( S \) of the circuit is defined as the maximum of spans of all its cones. For the above type of faults, it is sufficient to apply all possible patterns to each set of \( S \) consecutive flip-flops of the scan chain to guarantee coverage of all faults.

II. 3-WEIGHT WRBIST

The shift counter is an \((m+1)\) modulo counter, where \( m \) is the number of scan elements in the scan chain (since the generators are 9 bits wide, the shift counter has \([\log_2(9+1)]\)=4 stages). When the content of the shift counter is \( k \), where \( k=0,1,\ldots,8 \), a value for input \( p_k \) is scanned into the input of scan chain. The generator counter selects appropriate generators; when the content of the generator counter is \( i \), test patterns are generated by using \( \text{gen}(C) \), where \( i = 0,1,2 \).

![Fig. 3.1 Architecture of 3-Weight WRBIST](image-url)

Pseudo-random pattern sequences generated by an LFSR and a CA are modified (fixed) by controlling the AND and OR gates with overriding signals \( s_0 \) and \( s_1 \); fixing a random value to a 0 is achieved by setting \( s_0 \) to a 1 and \( s_1 \) to 0 and fixing a random value to a 1 is achieved by setting \( s_1 \) to a 1. Overriding signals \( s_0 \) and \( s_1 \) are driven by the outputs of \( T \) flip-flops, \( TF_0 \) and \( TF_1 \). The inputs of \( TF_0 \) and \( TF_1 \) are in turn driven by the outputs of the decoding logic \( D_0 \) and \( D_1 \), respectively, which are generated by the outputs of the shift counter and the generator counter as inputs. The shift counter is required by all scan-based BIST techniques and not particular to the proposed 3-weight WRBIST scheme. All BIST controllers need a pattern counter that counts the number of test patterns applied. The generator counter can be implemented from \([\log_2 G]\) MSB (most significant bit) stages of the existing pattern counter, where \( G \) is the number of generators, and no additional hardware is required for the generator counter. Hence, hardware overhead for implementing a 3-weight WRBIST is incurred only by the decoding logic and the fixing logic.
CONCLUSION

This paper presents a low hardware overhead TPG for scan based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with a reasonable length of test sequence. Unacceptably long test sequences are often required to attain high fault coverage with pseudorandom test patterns for circuits that have many random pattern resistant faults. The main objective of most recent BIST techniques has been the design of TPGs that achieve high fault coverage at acceptable test lengths for such circuits. While this objective still remains important, reducing heat dissipation during test application is also becoming an important objective. Since the correlation between consecutive patterns applied to a circuit during BIST is significantly lower, switching activity in the circuit can be significantly higher during BIST than that during its normal operation. Excessive switching activity during test application can cause several problems. The proposed TPG reduces the number of transitions that occur at scan inputs during scan shifting by scanning in the test patterns where neighboring bits are highly correlated. The proposed BIST is comprised of two TPGs: LT-RTPG and 3-weight WRBIST. Test sequences generated by the LT-RTPG detect easy-to-detect faults. Faults that escape LT-RTPG test sequences are detected by test patterns generated by the 3-weight WRBIST. The number of weight sets (generators) is minimized by guiding the proposed ATPG with cost functions that reflect the number of conflicting inputs to be incurred by setting an input to a binary value. An algorithm to design the 3-weight WRBIST that requires minimal hardware overhead and whose patterns cause minimal number of transitions during scan shift cycles is presented. Hardware overhead for the proposed TPG is further reduced by identifying compatible scan chains in multiple scan chain designs. To implement the LT-RTPG, LFSR and 3-Weight WRBIST. Combine all the three TPGs to get the best TPG for 100% fault coverage and minimum power dissipation using the VHDL language and Xilinx simulation tool. Future work of this project is to implement the 4-Weight WRBIST. The proposed BIST structure does not require modification of mission logic which can cause performance degradation. Experimental results for large industrial circuits demonstrate that the proposed TPG can significantly improve fault coverage of LFSR generated test sequences with low hardware overhead.

REFERENCES


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