Design Of Low Power 4bit Synchronous Counter Using Adiabatic Logic

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ABSTRACT—*This paper provides a design of low power 4bit synchronous counter. In the designing of VLSI circuits power dissipation has become a major concern. So by reducing power dissipations we can attain our low power circuit. We have different techniques so as to reduce these power dissipations. In our project, we adopt adiabatic logic so as to design the counter circuit. In Adiabatic circuit the charge stored in the load capacitor is recovered while in conventional CMOS it is transferred to the ground which is wastage of energy. The circuit used in this project is a 4-bit Synchronous counter. By implementing this circuit in adiabatic logic the power dissipation can be minimized compared to conventional CMOS. The design is implemented by using TANNER EDA tools.*

Keywords—Adiabatic logic, counter, power dissipation, D-flip-flop

I. INTRODUCTION

The power dissipation factor plays a critical role in VLSI designs especially in the high performance applications. These power dissipations are mainly of three types 1)Short circuit power dissipation 2)Leakage power dissipation 3)Dynamic switching power dissipation. In a logic circuit, whenever there is a direct flow of current exists between V_{DD} and ground it leads to Short circuit power dissipation. Leakage power dissipation is due to the sub threshold current in the transistor channel when it is turned off. Dynamic power dissipation refers to the power that is dissipated when the circuit inputs are high.

Adiabatic logic designs a circuit in such a way that it avoids the occurrence of the condition that both the PMOS and NMOS gets OFF and hence there will be no direct current flow between V_{DD} and GND by which we can avoid Short circuit power dissipation. Adiabatic computing decreases the Leakage power dissipation by restoring the energy at the nodes of the circuit. The power gating technique of adiabatic circuits which was done by shutting down the adiabatic units during idle states helps to reduce Dynamic power dissipation. Thus adiabatic logic circuits can achieve low power circuits by reducing all these kinds of power dissipations.[1,2,3]

II. RELATED WORK

CMOS technology which is the acronym of Complementary Metal Oxide Semiconductor Logic is designed by combining both PMOS and NMOS logics where PMOS design is referred as Pull up Network and the NMOS design is referred as Pull down Network. Leakage power dissipation is the major factor for the downfall of CMOS circuits, which can be overcome by adiabatic circuits. In a CMOS circuit when both PMOS and NMOS gets switched on there will be a direct path between V_{DD} and GND which is succeeded by the adiabatic logic circuits. Counter which was designed in both CMOS and Adiabatic logics when compared, we can observe that the CMOS counter utilizes more and more power than that of counter designed using adiabatic logic.[4,5]

III. PROPOSED METHOD

In this project we are designing a synchronous counter circuit using adiabatic logic. Counter is a digital circuit which is used for counting the pulses and it is the widest application of flip-flops. We are designing this counter in different logics of adiabatic such as ECRL, PFAL, 2PASCAL and these are as follows. So as to design a counter firstly we need to design a flip-flop and here, we are designing counter using D-flip-flop.

3.1. Design of ECRL counter

ECRL is the acronym of Efficient Charge Recovery Logic. It consists of four phases. First phase is Evaluation phase which utilizes the necessary power required for the circuit and hence the name pre charge phase. Second phase is the Hold phase which holds the power that it consumes in the Evaluation phase. Third phase is Recovery phase i.e., out and out/ returns its energy to the clk. Fourth phase is the wait phase which is used just to produce delay for another cycle.

The schematic diagram of D-flip-flop is as shown in Fig.1 and the counter that was designed using this D-flip-flop is as shown in Fig2.

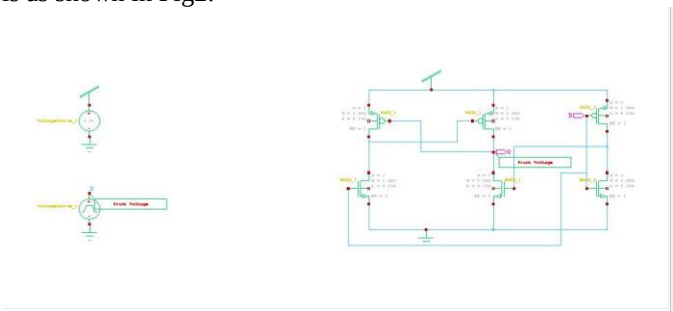

Fig1.schematic diagram of the D-flip-flop in ECRL

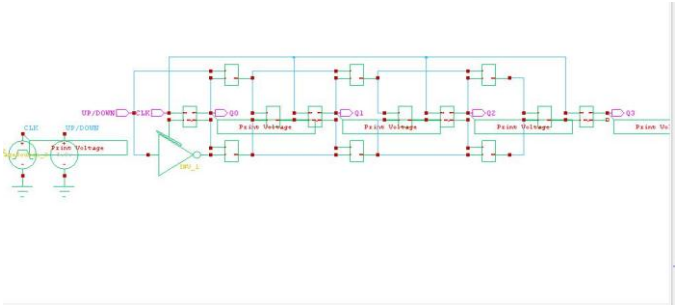

Fig2.schematic diagram of ECRL Counter

3.2 Design of PFAL Counter

PFAL is the acronym of Positive Feedback Adiabatic Logic. So as to improve the robustness against the technologies, in this logic we will use NMOS transistors between the output and power clock.

The schematic diagram of D-flip-flop in PFAL is as shown in Fig3.and the respective counter designed using this is as shown in Fig4.

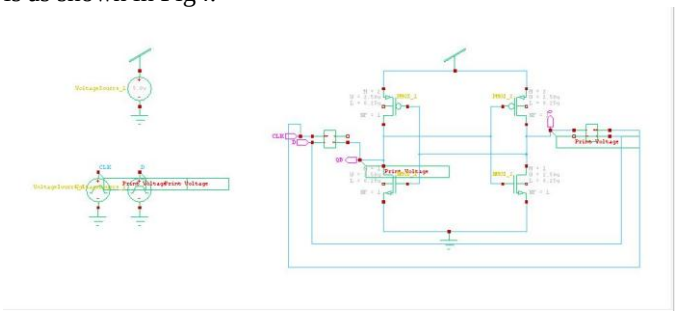

Fig3.schematic diagram of the D-flip-flop in PFAL

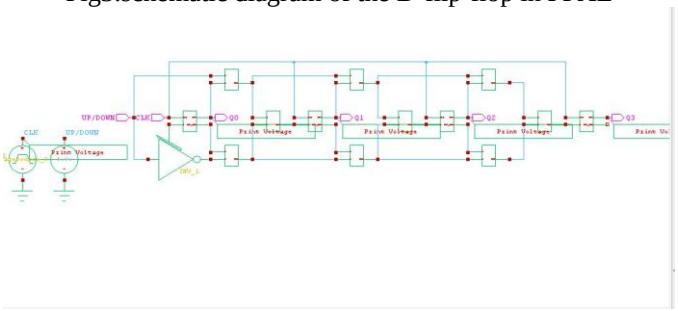

Fig4.schematic diagram of PFAL Counter

3.3. Design of 2PASCAL Counter

2PASCAL is the acronym of 2Phase Adiabatic Static Clocked Logic. It reduces dynamic switching activities compared to ECRL by reducing charging/discharging to occur after every clock cycle.

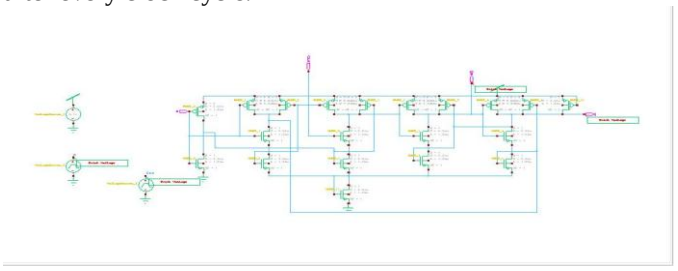

Fig5.schematic diagram of 2PASCAL D-flip-flop

The schematic diagram of D-flip-flop is as shown as shown in Fig5. and the counter designed with this D-flip-flop is as shown in Fig6. [6,7]

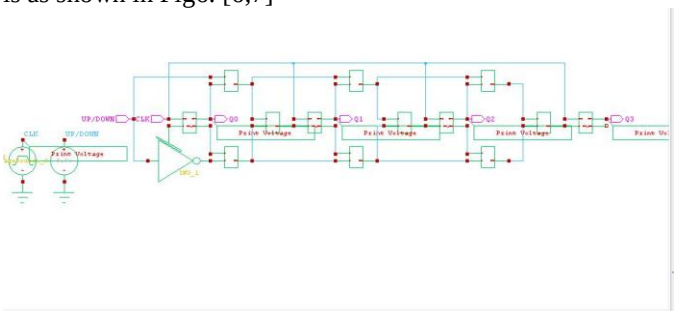

Fig6.schematic diagram of 2PASCAL Counter

Design of CMOS Counter

So as to observe the efficiency in power reduction by the adiabatic logic we have designed CMOS counter to compare the power results.

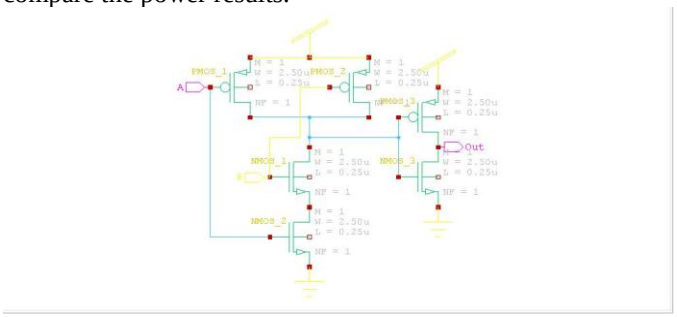

Fig7.schematic diagram of CMOS D-flip-flop

The schematic diagram of D-flip-flop in CMOS was as shown as in Fig7.and its respective counter that was designed was shown in Fig8.

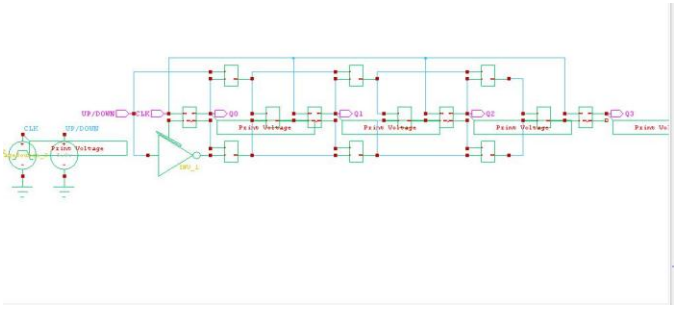

Fig8.shematic diagram of CMOS Counter

IV. RESULTS

The following table clearly shows the power dissipations of different logics which we have designed

Table 1: Comparison of results

S.NO.	KIND OF LOGIC	NO. OF TRANSISTORS	POWER UTILIZED
1.	CMOS	180	7.57*10^-2 watts
2.	ECRL	84	1.46*10^-2 watts
3.	PFAL	132	1.73*10^-2 watts
4.	2PASCAL	132	2.33*10^-2 watts

From the above table we can clearly say that the designing of counter with adiabatic logic has reduced power compared to that of the CMOS counter and thus we have attained our low power synchronous counter.

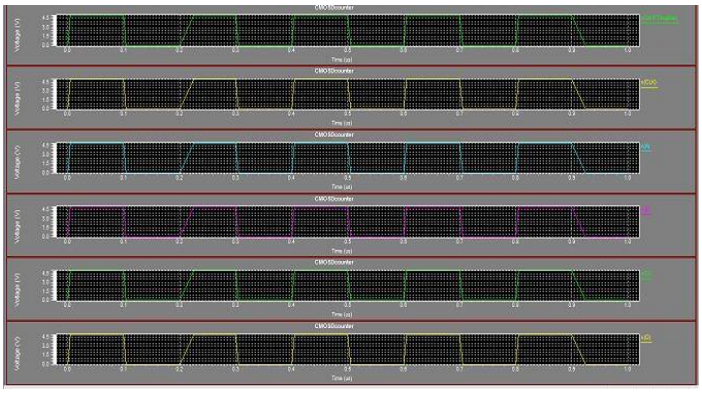

Fig9. Waveform result of a counter

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