Rational Sampling Rate Converter Design Analysis using Symmetric Technique

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Abstract — In this paper we proposed an efficient structure for sampling rate conversion by rational factor of L/M, where L is upsampling factor and M is downsampling factor. In this method, the coefficient symmetry of the linear phase filter is used. In this way, the number of required multiplications per output sample is reduced. For implementation we use linear phase FIR filter. The symmetric FIR filter has shown reduction in multipliers as compared to conventional polyphase implementation.

Keywords — *Multirate system, , linear phase, FIR filter, rational sampling rate conversion.*

I. INTRODUCTION

Sampling rate conversion is a process used to convert sampling rate of a signal from one rate to another. This technique is used in many applications like digital audio, communication systems, speech processing, radar systems, antenna systems etc. Sampling rates can be increased or decreased according to requirement. Increasing the sampling rate known as interpolation and decreasing the sampling rate is decimation. The multirate techniques are used to convert the given sampling rate to desired sampling rate and are called multirate system. The basic blocks of multirate system are interpolators and decimator. Combination of these blocks represent a system in which sampling rate is changed by a rational factor L/M. The block diagram of rational sampling rate converter is as follows:

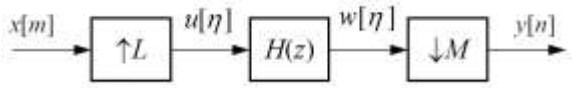


Fig. 1. Rational sampling-rate converter.

Fig. 1 shows that the input signal is upsampled by factor of L, after that signal is filtered by transfer function H(Z), and resulting signal is downsampled by a factor of M. A filter is used in between decimation and interpolation to suppress aliasing and to remove imaging respectively [2].

The relation between input sampling rate f_{in} and output sampling rate f_{out} is given by

$$f_{out} = \left(\frac{L}{M} \right) f_{in} \qquad (1)$$

$$H(z) = \sum_{k=0}^{N} h_k z^{-k} \qquad (2)$$

Where

$$h_{N-k} = h_k \qquad k = 0,1,\ldots,N \qquad (3)$$

H(z) is transfer function of linear phase FIR filter. Most of the cases, linear phase FIR filters are used. They are better than IIR filters because they have no feedback loops and can be implemented in a multirate system easily.

An efficient structure is proposed in [2] for implementing a linear-phase FIR filter of an order N for the sampling-rate conversion. In this method, the coefficient symmetry of the linear-phase filter is used in order to keep number of delays as low as possible. Optimized decimator has been presented to improve the implementation complexity [3]. The proposed decimator is implemented using Matlab as standard FIR, Half Band FIR and Nyquist FIR by using the multistage design techniques. The performance of different decimator designs is compared in terms of error and hardware requirements.

Design of sampling rate converter [4] based on least square method. Resampling realization method is used for better accuracy of signal resampling. Rational sampling rate conversion based on an FIR filter [5] can be used as a constant matrix multiplication which reduces arithmetic complexity compared with using MCM blocks.

GSM based digital down converter is proposed which uses optimal equiripple technique to reduce resource requirement and polyphase decomposition to improve hardware complexity and also reduces the pass band droop as well as increase the attenuation in folding band of CIC filter. A high speed interpolator using embedded LUT structure for software defined radios increases the speed and also save the resources [6]. For satellite data communication architecture for sampling rate converter is proposed in [7]. This design gives low system complexity and reduces power consumption. Polyphase implementation is shown in [8]. In this implementation multiplier are more than proposed one. FPGA based implementation of a multipliers less decimator is presented [9]. In paper [10] Number of required multiplications can be reduced. It partially utilizes the coefficient symmetry for linear phase prototype filter.

In this paper [11] an Interpolator has been designed and simulated. An area efficient method has been

presented to implement an interpolator for wireless communication systems.

Decimator design has been presented for multirate digital signal processing. It is observed from the simulated results that symmetric structure consumes almost 50% less multipliers and MPIS compared to transposed structure. So the symmetric structure based decimator in [12] is suitable to provide cost effective solution. Number of adders can be reduced by using Multiple constant multiplications [13]. This shows that MCM block with all coefficient using symmetric technique can reduce complexity without increasing storage elements. An efficient interpolator is designed for wireless communication systems [14]. For high speed and area efficient design multiplier less technique is used which substitutes multiply-and-accumulate operations with look up table (LUT) accesses.

Another method is used to reduce hardware complexity in [15]. It presents structures for sample rate conversion from compact disc (CD) to digital audio tape (DAT) and from DAT to CD. An efficient interpolator is designed for wireless communication systems [16]. Architecture is designed for sampling rate converter of the demodulator which is used for processing satellite data communication [17]. This design gives low system complexity and reduces power consumption and chip area requirements.

Another approach is presented in [18] which shows an optimized hardware to design & implement GSM based digital down convertor for **S**oftware **D**efined **R**adios. The proposed DDC is implemented using optimal equiripple technique is used to implement DDC to reduce the resource requirements.

High throughput Sample Rate Converters (SRC) finds applications Software Defined Radio (SDR) where a large degree of flexibility is required to support varied sample rates [19]. FIR filter is implemented using Transposed & Symmetric structure. The performance of two designs has been compared in terms of hardware requirements. Results show that symmetric structure has reduced hardware requirement as compared to Transposed structure [20].

An efficient multiplier-less technique is also presented in [21].It is basically designed for wireless applications like SDR and GSM. The Cascaded Integrator Comb decimation filter is used which performs sample rate conversion (SRC) utilizing only additions/subtractions. With the help of embedded LUTs of device, speed is increased. Different symmetrisation schemes are shown in [22]. Comparison shows that discrete time model gives better performance than continues time model. By designing frequency-response masking approach filters building the FB in such a way that the periodic filters are evaluated at the input sampling rate and the masking filters at the output sampling rate, the design and implementation complexity can be reduced when compared with other existing techniques [23]. Now a days VLSI technology is rising very fastly. The challenge of advanced VLSI technology is leakage in power consumption. This can be controlled by using different flip flop layouts [24]-[25].

This paper is divided into different sections as follows. Section II represents basic rational sampling rate converter. For simplicity, the coefficient symmetry of filter H(z) is not used but taken back into consideration in remaining paper. Section III gives design simulation. Design Analysis of the proposed method is given in section IV. Finally conclusion is given in section V.

II. RATIONAL SAMPLING RATE CONVERTER

This section shows, some relations for system in Fig 1. These relations are used in section 3 and 4 for generating an implementation structure for rational sampling rate converter. There are two parts in this section. First, time domain input output relation and second is compact matrix representation of input output relation. Matrix representation is more suitable to generate an efficient implementation [2].

A. *Basic input output relations between input and output samples*

For sampling rate converter shown in Fig 1, the time domain relations are given as

$$u[n]=\begin{cases} x\left[\dfrac{n}{L}\right] & for\ n=0,L,2L,\ldots \\ 0 & otherwise \end{cases} \tag{4}$$

$$w[n]=\sum_{k=0}^{N} h_k u[n-k] \tag{5}$$

$$y[n]=w[Mn] \tag{6}$$

Where hk's are coefficients of the transfer function H(z). The direct combination of (4)-(6) is following:

$$y[n]=\sum_{k=0}^{N} h_k x\left[\frac{Mn-k}{L}\right] \tag{7}$$

B. *Input-output relations in Matrix Form*

Based on (7), the (n+kL) th output sample, with k being an integer, is

$$\begin{aligned} y[n+KL] &= \sum_{k=0}^{N} h_k x\left[\frac{M(n+KL)-k}{L}\right] \\ &= \sum_{k=0}^{N} h_k x\left[\frac{Mn-k}{L}+KM\right] \end{aligned} \tag{8}$$

$$y[n+l]=\sum_{K_l=0}^{K_l^{\max}} h_{lM+(K_l-[lM/L])L}\, x\left[\frac{Mn}{L}-K_l+\left[\frac{lM}{L}\right]\right] \tag{9}$$

$$y[n+l]=\begin{bmatrix} h_{lM-[lM/L]L} \\ h_{lM-[lM/L]L+L} \\ \vdots \\ h_{lM+[(N-lM)/L]L} \end{bmatrix}^T \begin{bmatrix} x[m+\left\lfloor \frac{lM}{L} \right\rfloor] \\ x[m+\left\lfloor \frac{lM}{L} \right\rfloor -1] \\ \vdots \\ x[m-\left\lfloor \frac{(N-lM)}{L} \right\rfloor] \end{bmatrix} \quad (10)$$

For the rational sampling rate converter shown in fig (1) , L consecutive output samples, y[n+l] can be expressed as

$$y_{n,L} = H_{l\times(p+q+1)} x_{m+p,m-q} \quad (11)$$

Where $y_{n,L}$, $H_{L^*\ p+q+1}$, $\boldsymbol{p}$, $\boldsymbol{q}$ and $x_{m+p,m-q}$ are:

$$y_{n,L} = \begin{bmatrix} y[n] & y[n+1] & y[n+2] & ..... & y[n+L-1] \end{bmatrix}^T \quad (12)$$

$$H_{L^*(p+q+1)} = \begin{bmatrix} h_{-pL} & ... & h_{-L} & h_0 & h_L & ... & h_{(q-1)L} & h_{qL} \\ h_{M-pL} & ... & h_{M-L} & h_M & h_{M+L} & ... & h_{M+(q-1)L} & h_{M+qL} \\ h_{2M-pL} & ... & h_{2M-L} & h_{2M} & h_{2M+L} & ... & h_{2M+(q-1)L} & h_{2M+qL} \\ ... & ... & ... & ... & ... & ... & ... & ... \\ h_{(L-1)M-pL} & ... & h_{(L-1)M-L} & h_{(L-1)M} & h_{(L-1)M+L} & ... & h_{(L-1)M+(q-1)L} & h_{(L-1)M+qL} \end{bmatrix} \quad (13)$$

$$q=\lfloor N/L \rfloor \qquad p=\lfloor [(L-1)M]/L \rfloor \qquad h_k = 0,\ for\ k<0; k>N \quad (14)$$

$$x_{m+p,m-q} = \begin{bmatrix} x[m+p] & x[m+p-1] & ..... & x[m-q] \end{bmatrix}^T \quad (15)$$

C. Properties of Input Output Matrix $H_{L\times(p+q+1)}$

This section gives three important properties in the relationships between the elements in the matrix $H_{L\times(p+q+1)}$.

1) The p[th] column in the matrix contains following elements.

$$\tilde{h} = \begin{bmatrix} h_0 & h_M & h_{2M} & ..... & h_{(L-1)M} \end{bmatrix}^T \quad (16)$$

2) The l^{th} row in the matrix $H_{L\times\ p+q+1}$ for $l=0,1,...,L-1$ contains the $\mu_l^{\ th}$ polyphase component of the transfer function.

$$\mu_l = \mathrm{mod}(lM, L) \quad (17)$$

$\mu_l^{\ th}$ polyphase component with $\mu_\ell^{\ (b)}$ and $\mu_\ell^{\ (a)}$, they can be represented as

$$\mu_\ell^{\ (b)} = p - \left\lfloor \frac{\ell M}{L} \right\rfloor \quad (18)$$

$$\mu_\ell^{\ (a)} = q - \left\lfloor \frac{(N-\ell M)}{L} \right\rfloor \quad (19)$$

3) Matrix shown in (13) can be represented, as the coefficients of the Nth order transfer function H(z), as

$$H_{L\times(p+q+1)} = \begin{bmatrix} h_0^{(H)} & h_1^{(H)} & ... & h_l^{(H)} & ... & h_{L-1}^{(H)} \end{bmatrix}^T \quad (20)$$

Where

$$h_\ell^{\ H} = \begin{bmatrix} 0_{1,\mu_\ell^{(b)}} & h_{\mu\ell} & 0_{1,\mu_\ell^{(a)}} \end{bmatrix} \quad (21)$$

III. Design Simulation

This section shows how to efficiently utilize the coefficient symmetry of linear phase FIR filters.

A. Rational sampling rate conversion factor 2/3

This section shows rational sampling rate converter by a factor of L/M with L=2, M=3 and N=11. In this case output sampling frequency is decreased by 3/2 with respect to input sampling frequency.

$$\begin{bmatrix} y[n] \\ y[n+1] \end{bmatrix} = \begin{bmatrix} 0 & h_0 & h_2 & h_4 & h_6 & h_8 & h_{10} \\ h_1 & h_3 & h_5 & h_7 & h_9 & h_{11} & 0 \end{bmatrix} . x_{m+1,m-5} \quad (22)$$

By using coefficient symmetry of filter it can be rewritten as:

$$\begin{bmatrix} y[n] \\ y[n+1] \end{bmatrix} = \begin{bmatrix} 0 & h_0 & h_2 & h_4 & h_5 & h_3 & h_1 \\ h_1 & h_3 & h_5 & h_4 & h_2 & h_0 & 0 \end{bmatrix} . x_{m+1,m-5} \quad (23)$$

In order to generate a form that is appropriate for an efficient implementation the aforementioned equation is decomposed into four distinct parts as shown in eq. (24). First two terms can be implemented directly. Third term is called centro-symmetric matrix. It can be implemented by using decomposition shown in eq. (25):

$$\begin{aligned} c_0 &= (h_0 + h_3)/2 \\ c_1 &= (h_2 + h_5)/2 \\ d_0 &= (h_0 - h_3)/2 \\ d_1 &= (h_2 - h_5)/2 \end{aligned} \tag{26}$$

$$x^{2}_{m,m-4} = \begin{bmatrix} \mathrm{I}_2 & \mathrm{J}_2 \\ \mathrm{J}_2 & -\mathrm{I}_2 \end{bmatrix} \begin{bmatrix} x_{m,m-1} \\ x_{m-3,m-4} \end{bmatrix} \tag{27}$$

$$\begin{bmatrix} y\ n \\ y\ n+1 \end{bmatrix} = h_4 x\ m-2 \begin{bmatrix} 1 \\ 1 \end{bmatrix} + h_1 x\ m-5 \begin{bmatrix} 1 \\ 0 \end{bmatrix} + h_1 x\ m+1 \begin{bmatrix} 0 \\ 1 \end{bmatrix} + \begin{bmatrix} h_0 & h_2 & h_5 & h_3 \\ h_3 & h_5 & h_2 & h_0 \end{bmatrix} \begin{bmatrix} x_{m,m-1} \\ x_{m-3,m-4} \end{bmatrix} \tag{24}$$

$$\begin{bmatrix} h_0 & h_2 & h_5 & h_3 \\ h_3 & h_5 & h_2 & h_0 \end{bmatrix} \begin{bmatrix} x_{m,m-1} \\ x_{m-3,m} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} c_1 & c_2 & 0 & 0 \\ 0 & 0 & d_2 & d_1 \end{bmatrix} x^{2}_{m,m-4} \tag{25}$$

The implementation structure for 2/3 factor is given in Fig. 2. For generating y[n] and y[n+1], this structure requires 7 multiplications and 12 additions. This means it requires 3.5 multiplications and 6 additions per output sample. Same system without utilizing the coefficient symmetry, requires 6 multiplications and 5 additions per output sample.

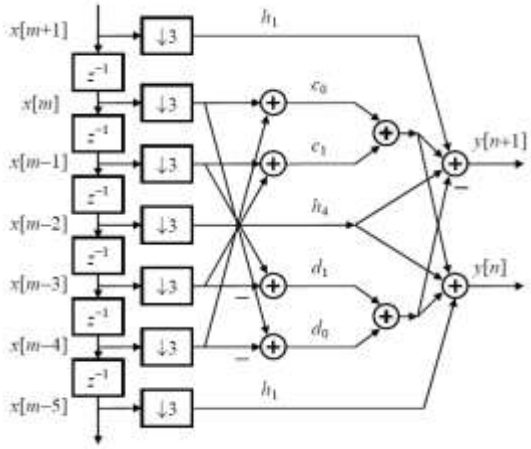


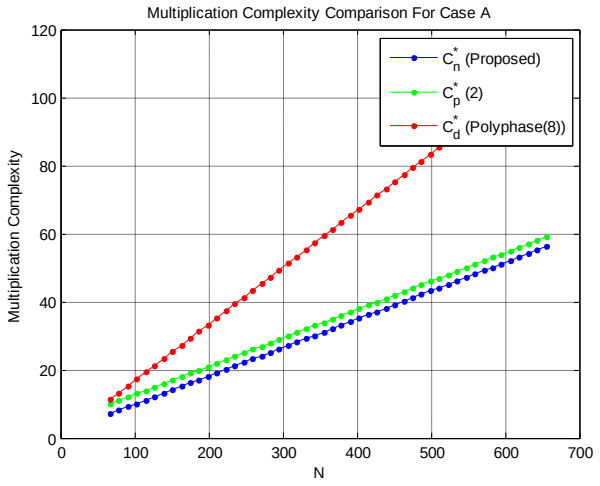
FIG.2 IMPLEMENTATION STRUCTURE FOR A RATIONAL SAMPLING-RATE CONVERTER BY A FACTOR OF 2/3

IV. DESIGN ANALYSIS

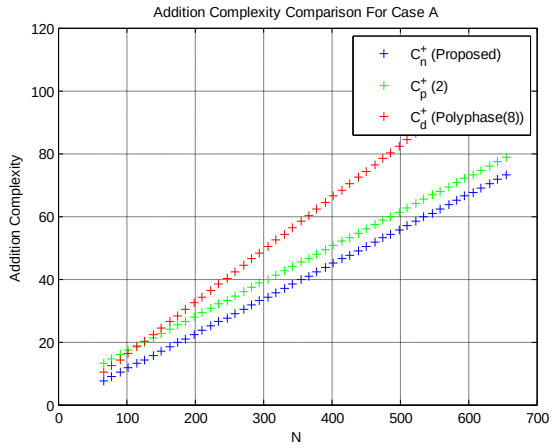
This section shows that how proposed method is better than existing ones. As seen in figure 3, the proposed method gives results having low implementation complexity as compare to polyphase implementation. Results show that when the filter order is increased then complexity is decreased. Table I shows that proposed method results in a system with lower implementation complexity compared with polyphase [8] and paper [2].

TABLE I

	Proposed		Paper [2]		Polyphase[8]	
N	**Cn***	**Cn+**	**Cp***	**Cp+**	**Cd***	**Cd+**
211	19.16	23.667	22.00	29.33	35.33	34.33
214	19.167	23.667	22.50	30.33	35.83	34.33
23	3.167	2.333	4.50	7.00	4.00	3.00
209	18.667	23.00	19.833	32.667	35.00	34.00
210	19.167	23.667	20.833	31.00	35.167	34.167
212	19.167	23.667	20.633	33.733	35.50	34.50



(a)



(b)

Fig. 3 Implementation complexity for rational sampling rate converters by 6/11 for case A(i.e. N=M(L-1)+(2k+1)L) (a) Number of multiplications(C*) per output sample. (b) Number of additions(C+) per output sample

V. CONCLUSION

In this paper an efficient structure is designed for sampling rate converter having rational factor L/M. The proposed implementation shows reduced number of multiplications per output sample as compare to polyphase implementation. Finally the implementation complexity of proposed approach is evaluated and with the help of some examples, efficiency of the proposed implementation is compared with others.

REFERENCES

[1] R. E. Crochiere and L. R. Rebiner, Multirate Digital Signal Processing. Englewood Cliffs, NJ:Prentice-Hall, 1983.

[2] Robert Bregovic, Ya JunYu, Tapio Saramaki, " Implementation of Linear-Phase FIR Filters for a Rational Sampling-Rate Conversion Utilizing the Coefficient Symmetry", IEEE Transactions on circuits and systems, Vol. 58, No. 3, pp. 548-561, MARCH 2011.

[3] Rajesh Mehra and Swapna Devi, "Optimized Design of Decimator for Alias Removal in Multirate DSP applications", Nonlinear System and Wavelet Analysis, pp. 100-103, 2010.

[4] Yu Huijun, "Design Of A Sample-Rate Converter Based On Least-Square Method", IEEE International Conference on computer science and Information processing, pp. 332-335, June 2012.

[5] Oscar Gutafsson and Hakan Johanson, "Efficient Implementation of FIR Filter Based Rational Sampling Rate Converters Using Constant Matrix Multiplication", IEEE International Conference on signals, systems and computers, pp. 888-891, 2006.

[6] Rajesh Mehra, Swapna Devi, "FPGA Based Design of High Performance Decimator using DALUT Algorithm", ACEEE International Journal on Signal and Image Processing, Volume 1, pp. 9-13, 2010.

[7] K. R. Nataraj, Dr S. Ramachandran and Dr B. S. Nagabushan, " Design of Architecture for Sampling Rate Converter of demodulator", IEEE International Conference on Computer and Electrical Engineering, Vol. 2, pp. 427-430, 2009.

[8] C-C Hasiao, "Polyphase filter matrix for rational sampling rate conversion", IEEE International Conference on Speech, Signal Process, pp. 2173-2176, April 1987.

[9] Rajesh Mehra and Lajwanti, "FPGA based speed efficient decimator using distributed arithmetic algorithm", Internatinal Journal of Computer Application, Vol 80, No. 11, Oct 2013.

[10] Robert Bregovic, Ya Jun Yu and Ari Viholainen, "Implementation of Linear-Phase FIR Nearly Perfect Reconstruction Cosine-Modulated Filter banks Utilizing the Coefficient Symmetry", IEEE Transactions on circuits and systems, Vol. 57, No. 1, pp. 139-151, January 2010.

[11] Rajesh Mehra and Shailly Verma, "Area Efficient Interpolator Using Half-Band Symmetric Structure" International Journal of Recent Technology and Engineering ISSN: 2277-3878, Volume-1, Issue-6, January 2013.

[12] Rajesh Mehra, and Lajwanti Singh, "cost analysis and simulation of decimator for multirate applications," International Journal of Computers & Technology, vol. 11, no. 1, pp.2175-2181, 2013

[13] Ya Jun Yu, Dong Shi and Robert Bregovic, "On the Complexity Reduction of Polyphase Linear Phase FIR Filters with Symmetric Coefficient Implementation", IEEE International Conference on circuits and systems, pp. 277-280, 2009.

[14] Rajesh Mehra and Ravinder kaur, "Reconfigurable Area and Speed Efficient Interpolator using DALUT Algorithm", Advanced in Networks and Communications, Volume 132, pp.117-125, 2011.

[15] Mahdi Mottaghi-Kashtiban, Saeed Farazi, and Mahrokh G. Shayesteh, "Optimum Structures for Sample Rate Conversion from CD to DAT and DAT to CD Using Multistage Interpolation and Decimation", IEEE International Symposium on Signal Processing and Information Technology, pp. 633-637, 2006.

[16] Rajesh Mehra , "FPGA Design of Optimized CIC Interpolator for DSP Based Wireless Communication System", IMS MANTHAN Journal of Mgt., Computer Science and Journalism, Volume 5, Issue-2, pp. 43-46, 2010

[17] K.R.Nataraj, Dr. S. Ramachandaran and dr. B. S. Nagabhushan, "Design of architecture of sampling rate converter of demodulator", IEEE International Conference on computer and electrical engineering, pp. 351-355, 2009.

[18] Rajesh Mehra and Swapna Devi, "Efficient Hardware Co-Simulation of Down Converter for Wireless Communication Sysrems", International Journal of VLSI Design and communication Systems, Volume 1, No.2.,June 2010.

[19] Jeffrey P. Long and Jose A. Torres, " High Throughput Farrow Re-samplers Utlizing Reduced Complexity FIR Filters", IEEE International Conference on military communication, pp. 1-6, 2012.

[20] Rajesh Mehra and Kanupriya, "Area efficient design of FIR filter using symmetric structure", International Journal of Advanced Research in Computer and communication engineering, Vol 1, Issue 10, pp. 842-845, Dec 2012.

[21] Rajesh Mehra and Rashmi Arora, "FPGA-Based Design of High Speed CIC Decimator for Wireless Applications", International Journal of Advanced Computer Science and Applications, Vol. 2, No.5 ,2011.

[22] Vesa Lehtinen, Djordje Babic and Markku Renfors, " On impulse Response Symmetry of farrow interpolators in Rational Sample Rate Converter", IEEE Conference on control, communication and signal processing, pp.693- 696, 2004.

[23] Bregovic, Yong Ching Lim, Saramaki, "Frequency Response Masking Based Design of Two-Channel FIR Filterbanks with Rational Sampling Factors and Reduced Implementation Complexity", IEEE International Conference on Image and Signal Processing and Analysis, pp. 121-126, 2005.

[24] Rajesh Mehra and Neha Thapa, "Power and area analysis of flip flop using different techniques", International Journal of Computer trends and Technology,Vol. 24, No.2, pp. 57-62, June 2015.

[25] Rajesh Mehra and Avneet Kaur, " Enhancement of SR Flip Flop Layout design in 45nm technology", International Journal of Computer trends and Technology, Vol 25, No.3, pp. 118-122, 2015.